QD01/D
DISK CONTROLLER
TECHNICAL MANUAL
(MSCP COMPATIBLE)

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WARNING

This equipment generates, uses and can radiate radio frequency energy, and if not installed and used in accordance with the technical manual, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of Federal Communications Commission (FCC) Rules, which are designed to provide reasonable protection against such interference when operating in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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EMULEX PRODUCT WARRANTY

CONTROLLER WARRANTY: Emulex warrants for a period of twelve (12) months from the date of shipment that each Emulex controller product supplied shall be free from defects in material and workmanship.

CABLE WARRANTY: All Emulex provided cables are warranted for ninety (90) days from the time of shipment.

The above warranties shall not apply to expendable components such as fuses, bulbs, and the like, nor to connectors, adaptors, and other items not a part of the basic product. Emulex shall have no obligation to make repairs or to cause replacement required through normal wear and tear or necessitated in whole or in part by catastrophe, fault or negligence of the user, improper or unauthorized use of the product, or use of the product is such a manner for which it was not designed, or by causes external to the product, such as but not limited to, power failure or air conditioning. Emulex's sole obligation hereunder shall be to repair or replace any defective product, and, unless otherwise stated, pay return transportation cost for such replacement.

Purchaser shall provide labor for removal of the defective product, shipping charges for return to Emulex and installation of its replacement. THE EXPRESSED WARRANTIES SET FORTH IN THIS AGREEMENT ARE IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED OR IMPLIED, INCLUDING WITHOUT LIMITATION, ANY WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, AND ALL OTHER WARRANTIES ARE HEREBY DISCLAIMED AND EXCLUDED BY EMULEX. THE STATED EXPRESS WARRANTIES ARE IN LIEU OF ALL OBLIGATIONS OR LIABILITIES ON THE PART OF EMULEX FOR DAMAGES, INCLUDING BUT NOT LIMITED TO SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES ARISING OUT OF, OR IN CONNECTION WITH THE USE OR PERFORMANCE OF THE PRODUCT.

RETURNED MATERIAL: Warranty claims must be received by Emulex within the applicable warranty period. A replaced product, or part thereof, shall become the property of Emulex and shall be returned to Emulex at Purchaser's expense. All returned material must be accompanied by a RETURN MATERIALS AUTHORIZATION (RMA) number assigned by Emulex.

Section 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

The QD01/D Disk Controller, designed and manufactured by Emulex Corporation, is a MSCP-compatible controller with a ST-506 peripheral interface. This manual is designed to help you install and use your QD01/D Disk Controller in the most efficient and straightforward manner possible. The contents of the eight sections and four appendices are described briefly below.

Section 1	**General Description:** This section contains an overview of the QD01/D Disk Controller.
Section 2	**Controller Specification:** This section contains the specification for the QD01/D Disk Controller.
Section 3	**Planning the Installation:** This section contains the information necessary to plan your installation.
Section 4	**Installation:** This section contains the information needed to set up and physically install the subsystem.
Section 5	**Troubleshooting:** This section describes fault isolation procedures that can be used to pinpoint trouble spots.
Section 6	**Registers and Programming:** This section contains a description of the subsystem's LSI-11 bus registers and an overview of the Mass Storage Control Protocol (MSCP).
Section 7	**Functional Description:** This section describes the controller architecture.
Section 8	**Interfaces:** This section describes the subsystem LSI-11 bus and ST-506 interfaces.
Appendix A	**Autoconfigure, CSR and Vector Addresses:** This appendix contains a description of the DEC algorithm for the assignment of CSR addresses and vector addresses.
Appendix B	**PROM Removal and Replacement:** This appendix contains PROM removal and replacement instructions to allow the user to upgrade the QD01/D Disk Controller in the field.
Appendix C	**Utilities and Diagnostics:** This appendix contains a list of the utilities and diagnostics that are applicable to the QD01/D.
Appendix D	**Disk Drive Configuration Parameters:** This appendix contains configuration parameters for common ST-506 disk drives.

1.2 SUBSYSTEM OVERVIEW

The QD01/D Disk Controller connects high-capacity mass storage peripherals to LSI-11 computers manufactured by Digital Equipment Corporation (DEC). The QD01/D implements DEC's Mass Storage Control Protocol (MSCP) to provide a software-transparent interface for the host DEC computer. To provide traditional Emulex flexibility in peripheral selection, the QD01/D uses the versatile, industry standard ST-506 interface as its peripheral interface. The ST-506 interface is used on 5.25-inch Winchester disk drives built by a large number of manufacturers.

1.2.1 MASS STORAGE CONTROL PROTOCOL (MSCP)

MSCP is a software interface designed to lower the host computer's mass storage overhead by offloading much of the work associated with file management into an intelligent mass storage subsystem. In concert with ST-506 compatible peripherals, the QD01/D provides just such a subsystem. The QD01/D relieves the host CPU of many file maintenance tasks. The QD01/D Disk Controller performs these MSCP functions: error checking and correction, bad block replacement, seek optimization, command prioritizing and ordering, and data mapping.

This last feature is, perhaps, the most important. This feature allows the host computer's operating system software to store data in logical blocks that are identified by simple logical block numbers (LBNs). Thus, the host does not need to have detailed knowledge of the peripheral's geometry (cylinders, tracks, sectors, etc.). This feature also makes autoconfiguration a simple matter. During system start-up, the host operating system queries the subsystem to find its capacity (the number of logical blocks that the subsystem can store).

Because the host operating system does not need to have detailed knowledge of its mass storage subsystem, the complexity of the operating system itself has been reduced. This reduction comes about because only one or two software modules are required to allow many different subsystems to be connected to a host.

1.3 PHYSICAL ORGANIZATION OVERVIEW

The QD01/D Disk Controller is a modular, microprocessor-based disk controller that connects directly to the host computer's LSI-11 bus backplane. The microprocessor architecture ensures excellent reliability and compactness.

The QD01/D is contained on a single dual-wide printed circuit board assembly (PCBA) that plugs directly into an LSI-11 bus backplane slot.

The QD01/D supports up to two physical or four logical disk drives. Aggregate data storage capacities are limited only by the capacities of the peripherals. Figure 1-1 shows one possible ST-506 configuration.

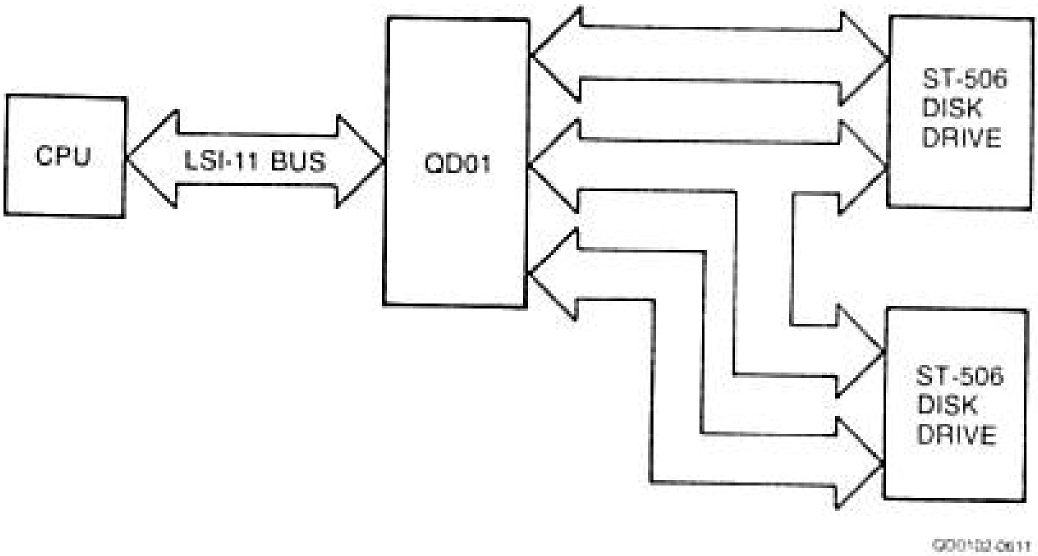

Figure 1-1. QD01/D Subsystem Configuration

1.4 SUBSYSTEM MODELS and OPTIONS

The QD01/D Disk Controller, with appropriate peripherals, provides a DEC MSCP-compatible mass storage subsystem. The QD01/D is pictured in Figure 1-2. The QD01/D is identified by a top level assembly tag that is glued to the 8031 microprocessor chip on the PWB. The QD01/D top level assembly number is given in Table 1-1 along with the part numbers of the items that are delivered with the QD01/D.

Table 1-1. Basic Subsystem Contents

Itm	Qty	Description	Part Number
1	1	QD01/D Disk Controller	QD0110202
2	1	22-Bit Addressing Kit	QD0113002
3	1	QD01/D Technical Manual	QD0151002

1.4.1 SUBSYSTEM OPTIONS

Table 1-2 lists the options that can be ordered to tailor your QD01/D to your particular application. Software programs are offered in distribution kits that include media and documentation.

Table 1-2. Subsystem Options

Option	Description
PX995180n-0n[1]	Includes the Emulex PDP/LSI MSCP Formatter Program (SXMX8A). Distribution kit is per customer order.
VX9951804	Includes the Emulex MicroVAX QD01/D MSCP Disk Formatter Program (FQD01M).
QD0113003	QD01 Cabling Kit MICRO/PDP-11 and MicroVAX I and II Tower. Includes cables, panels, and instructions.
QU0111201-0n[2]	34-line, control interface cable for ST-506 disk drives. Cable length is per customer order.
QU0111202-0n[2]	20-line, data interface cable for ST-506 disk drives. Cable length is per customer order.
QU0111203-0n[2]	34-line, daisy-chain control interface cable for ST-506 disk drives. Cable length is per customer order.

[1] See Appendix C for distribution kit part numbers.

[2] See Table 4-5 for part numbers for specific cable lengths.

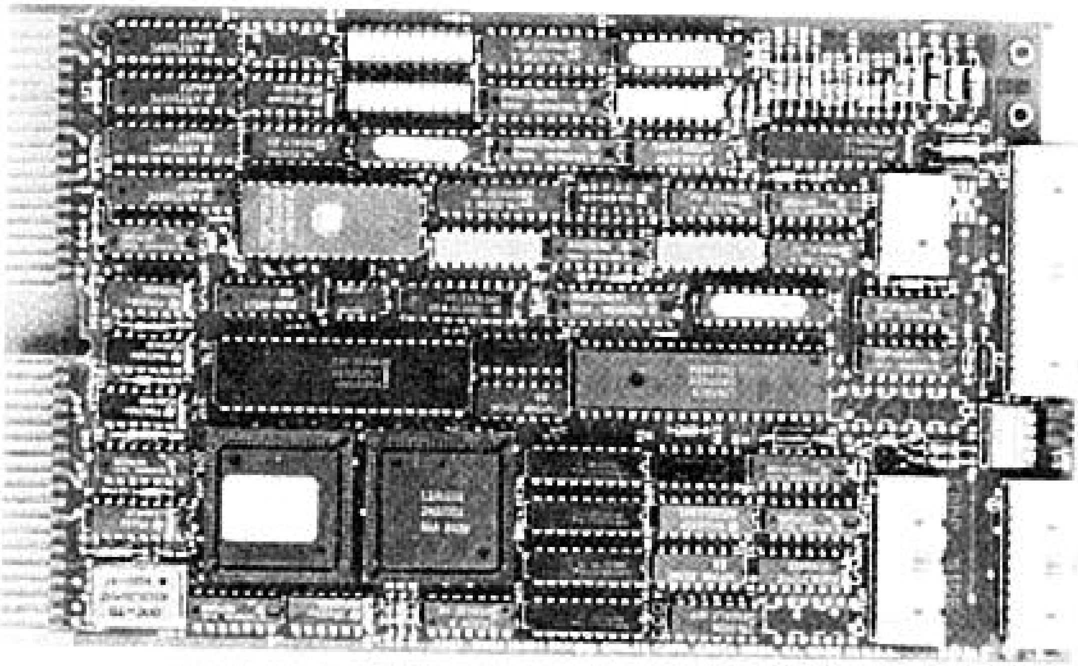

Figure 1-2. QD01/D Disk Controller

Options are specified as separate line items on a sales order. An example of an actual sales order is shown in Figure 1-3.

Item	Qty	Model Number	Comment/Description
1.	1	QD01/D	Disk Controller implementing DEC MSCP with ST-506 drives.
2.	1	QU0111201-04	Control interface cable for ST-506 drives, 12 ft
3.	2	QU0111202-04	Data interface cable for ST-506 drives, 12 ft
4.	1	QU0111203-04	Daisy-chain control interface cable for ST-506 drives, 4 ft

Figure 1-3. Sales Order Example

1.5 FEATURES

The following features enhance the usefulness of the QD01/D Disk Controller.

1.5.1 MICROPROCESSOR DESIGN

The QD01/D design incorporates an eight-bit, high-performance CMOS microprocessor to perform all controller functions. The microprocessor approach provides a reduced component count, high reliability, easy maintainability, and the microprogramming flexibility that allows MSCP to be implemented without expensive, dedicated hardware.

1.5.2 CONFIGURATION FLEXIBILITY

The QD01/D Disk Controller provides complete configuration flexibility. It supports two physical (four logical) ST-506 compatible disk drives of various types and capacities. The user can specify many different drive configurations by using the QD01/D's Nonvolatile Random Access Memory (NOVRAM). The QD01/D NOVRAM supports two, ST-506 drive interfaces. In addition, the user can change these stored subsystem configurations by altering the NOVRAM using Emulex software or the QD01/D's extended command set. The flexibility of the QD01/D configuration NOVRAM eliminates the need for special configuration PROMs and field upgrade kits.

1.5.3 SELF-TEST

The QD01/D incorporates an internal self-test routine. This test exercises all parts of the microprocessor, the on-board memory, the LSI-11 bus interface, and the ST-506 interface. Although this test does not completely test all circuitry, successful execution indicates a very high probability that the disk controller is operational. If the QD01/D fails the self-test, it leaves three light-emitting diodes (LEDs) ON and sets an error bit in the Status and Address (SA) register (base address plus 2).

1.5.4 SEEK OPTIMIZATION

The QD01/D is able to pool the various seeks that need to be performed and determine the most efficient order in which to do them. This is an especially important feature in heavily loaded systems. The disk controller's ability to arrange seeks in the optimum order saves a great deal of time and makes the entire system more efficient.

1.5.5 COMMAND BUFFER

The QD01/D contains a buffer that is able to store 13 MSCP commands. This large buffer allows the subsystem to achieve a higher throughput and to operate at a very efficient level.

1.5.6 ADAPTIVE DMA

During each DMA data transfer burst, the QD01/D monitors the LSI-11 bus for other pending DMA requests and suspends its own DMA activity to permit other DMA transfers to occur. The host processor programs the DMA burst length during the MSCP initialization sequence or the QD01/D defaults to 16 words per burst. In addition, the QD01/D firmware design includes a switch selectable DMA burst delay to avoid data late conditions. Because of these adaptive DMA techniques, the QD01/D ensures that CPU functions, including interrupt servicing, are not locked out for excessive periods of time by high-speed disk transfers.

1.5.7 ERROR CONTROL

The disk controller presents error-free media to the operating system by correcting soft errors and retrying operations without intervention by the host.

1.5.8 BLOCK-MODE DMA

The QD01/D supports block-mode DMA for accessing memory. In this mode, the initial address of the data is transmitted, followed by a burst of up to 16 words of data. The memory address is automatically incremented to accommodate this burst. Block mode transfers considerably reduce the overhead associated with DMA operations.

1.5.9 TWENTY-TWO-BIT ADDRESSING

The QD01/D supports full 22-bit addressing to utilize the full capacity of the expanded LSI-11 bus.

1.6 COMPATIBILITY

1.6.1 DIAGNOSTICS

Emulex offers diagnostic programs to support the use and maintenance of the QD01/D. For PDP/LSI systems, Emulex offers the Emulex PDP/LSI MSCP Formatter Program (SXMX8A). For MicroVAX systems, Emulex offers the MicroVAX QD01/D MSCP Disk Formatter Program (FQD01M).

1.6.2 OPERATING SYSTEMS

The QD01/D implements MSCP. Emulex supports its implementation of MSCP beginning with the indicated version of the following DEC operating systems:

Operating System	Version
Micro/VMS	4.0
RSTS/E	8.0
RSX-11M	4.1
RSX-11M-PLUS	2.1
RT-11	5.1

1.6.3 HARDWARE COMPATIBILITY

The QD01/D Disk Controller complies with DEC LSI-11 bus protocol, and it directly supports 22-bit addressing and block-mode DMA. The QD01 also supports scatter-write and gather-read operations on the MicroVAX I.

The disk drives supported by the QD01/D are not media compatible with comparable DEC MSCP products.

ST-506 disk drives that are supported by the QD01/D should provide buffered head stepping. Buffered stepping is required to provide adequate performance in DEC operating environments. (See subsection 6.3.1.1.1 for more information on step code.)

1.7 PERFORMANCE

The QD01/D Disk Controller provides performance superior to that of DEC MSCP mass storage subsystems for the LSI-11 bus. The QD01/D allows the user to select from a wide range of low-cost peripherals that, when combined with the QD01/D, provide very cost-effective solutions to mass storage on LSI-11 bus based computer systems.

2.1 OVERVIEW

This section contains the general, environmental, physical, electrical, and port specifications for the QD01/D Disk Controller. Specifications are contained in tables, and the tables are oriented around areas of interest as listed below:

Subsection	Title
2.2	General Specification
2.3	Environmental Specification
2.4	Physical Specification
2.5	Electrical Specification

2.2 GENERAL SPECIFICATION

A general specification for the QD01/D Disk Controller is contained in Table 2-1.

Table 2-1. QD01/D Disk Controller General Specifications

Parameter	Description
FUNCTION	Providing mass data storage to Digital Equipment Corporation (DEC) computers that use an LSI-11 bus
Logical CPU Interface	Emulates DEC's Mass Storage Control Protocol (MSCP)
Diagnostic Software	Emulex PDP/LSI MSCP Disk Formatter Program (SXMX8A or a more recent revision), MicroVAX QD01 MSCP Disk Formatter Program (FQD01M)
Operating System Compatibility	Micro/VMS V4.0 and above RSTE/S V8.0 and above RSX-11M V4.1 and above RSX-11M PLUS V2.1 and above RT-11 V5.1 and above

(continued on next page)

Table 2-1. QD01/D Disk Controller General Specifications (continued)

Parameter	Description
CPU I/O Technique	Direct Memory Access, including Adaptive Techniques and Block Mode; supports scatter-write and gather-read on the MicroVAX I
INTERFACE	
CPU Interface	Extended LSI-11 bus interface
Device CSR Address	
Standard	17772150_8
Alternates	~~17772154_8~~ 17760334_8 17760340_8 17760344_8 17760350_8 17760354_8 17760360_8
Vector Address	Programmable
Priority Level	BR4 and BR5
Bus Loading	1 DC Load, 2.5 AC Loads
Peripheral Interface	Seagate Technology ST-506
Number of Physical Drives Supported	2
Maximum Cable Length	20 feet (ft) 6 meters (m)
Step Pulse Interval	Programmable, 3 msec to 12 usec[1]

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[1] For adequate performance under DEC operating systems, Emulex recommends using a disk drive that can buffer step pulses. (See subsection 6.3.1.1.1 for more information on step code.)

2.3 ENVIRONMENTAL SPECIFICATION

Table 2-2 contains the environmental specifications for the QD01/D Disk Controller.

Table 2-2. QD01/D Disk Controller
Environmental Specifications

Parameter	Description
OPERATING TEMPERATURE	10°C (50°F) to 40°C (104°F), where maximum temperature is reduced 1.8°C per 1000 meters (1°F per 1000 feet) altitude
RELATIVE HUMIDITY	10% to 90% with a maximum wet bulb of 28°C (82°F) and a minimum dewpoint of 2°C (3.6°F)
COOLING	6 cubic feet per minute
HEAT DISSIPATION	82 BTU per hour

2.4 PHYSICAL SPECIFICATION

Table 2-3 contains the physical specifications for the QD01/D Disk Controller.

Table 2-3. QD01/D Disk Controller
Physical Specifications

Parameter	Description
PACKAGING	Single, dual-wide, four-layer PCBA
Dimensions	5.186 by 8.70 inches 13.172 by 22.09 centimeters (see Figure 2-1)
Shipping Weight	3 pounds

2.5 ELECTRICAL SPECIFICATION

Table 2-4 lists and describes the electrical specification for the QD01/D Disk Controller.

Table 2-4. QD01/D Disk Controller
Electrical Specifications

Parameter	Description
POWER	5 VDC ± 5%, 2.6 amperes (A)

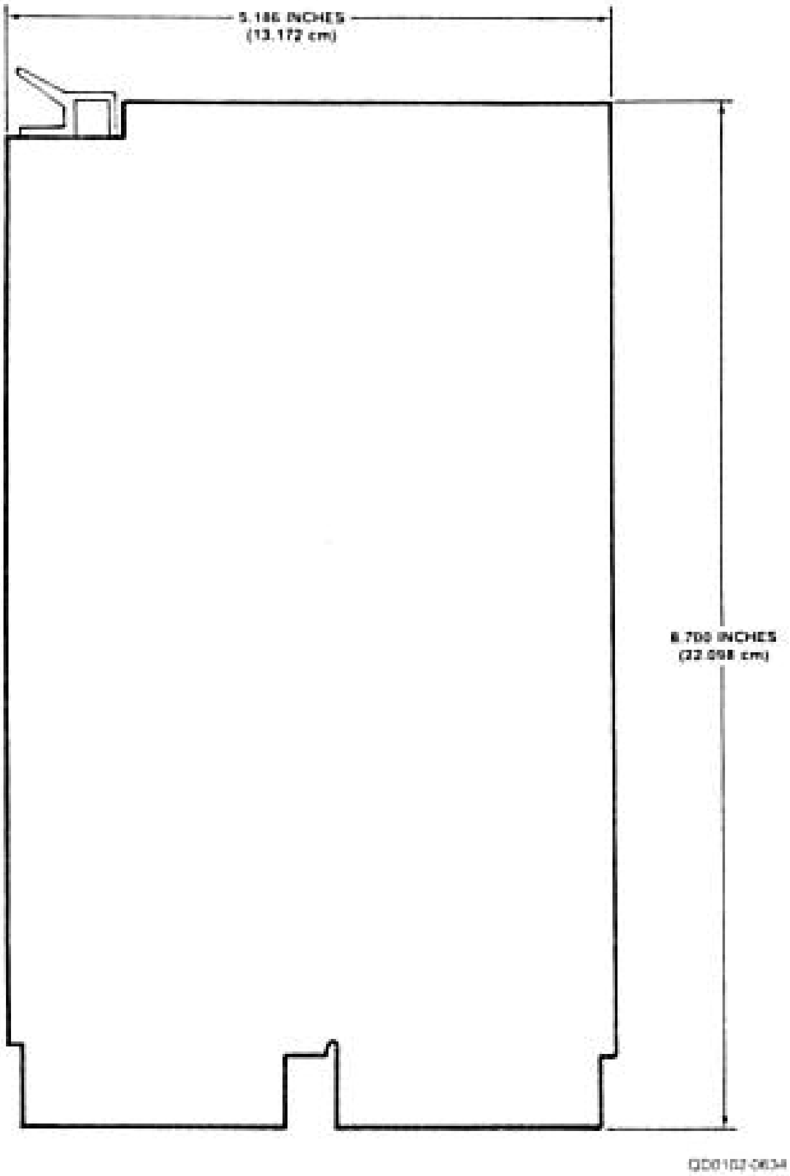

Figure 2-1. QD01/D Disk Controller Dimensions

Section 3
PLANNING THE INSTALLATION

3.1 OVERVIEW

This section is designed to help you plan the installation of your QD01/D Disk Controller. Taking a few minutes and planning the configuration of your subsystem before beginning its installation will result in a smoother installation with less system down time. As a planning tool, this section explains some of the practical matters that need to be considered before you begin your installation.

This section contains QD01/D application examples and configuration procedures. The subsections are listed in the following table:

Subsection	Title
3.2	MSCP Subsystem Configuration
3.3	A DEC MSCP Subsystem
3.4	The QD01/D MSCP Subsystem
3.5	Operating Systems, Device and Vector Addresses

Following the procedures contained in these subsections will help you get the most from your QD01/D Disk Controller.

3.1.1 CONFIGURATION DEFINED

As used in the computer industry, the term **configuration** is generally used to define the physical and logical arrangement of a system, or put another way, the manner in which the parts of a system relate to one another.

When used this way, the word configuration has quite a number of implications: size (capacity, speed, bandwidth), cabling (what is hooked to what), logical arrangement (which functions are combined on which components), location (bus slot, local/remote, bus address, vector, unit address), and so on.

Many of these factors can be affected by the user, either through the use of switches or by cabling the system appropriately. In other words, the configuration, and thus the function, of a system is defined and determined by the user.

3.2 MSCP SUBSYSTEM CONFIGURATION

The following paragraphs describe MSCP Subsystem concepts, including architecture, unit numbering, capacities, and related concepts.

3.2.1 ARCHITECTURE

MSCP is a protocol designed by DEC for mass storage subsystems using Digital Storage Architecture (DSA). In a MSCP mass storage subsystem, DSA comprises three functional and physical layers:

- **Host Layer.** An MSCP class-driver in the host system receives requests from the operating system and then relays data and commands to the controller in MSCP message packets.
- **Controller Layer.** The MSCP controller communicates with both the host layer and the mass storage layer. The controller transmits MSCP message packets to and from the host MSCP class-driver and performs data-handling functions for the mass storage devices. The QD32/D functions as the controller layer.
- **Mass Storage Layer.** The mass storage peripheral devices communicate with the MSCP controller and send or receive data as specified by the MSCP controller.

MSCP defines the form of the message packets that are exchanged by the host and the MSCP controller. The QD01/D implements MSCP in mass storage subsystems using ST-506 as the peripheral interface.

3.2.2 PERIPHERAL NUMBERING

Each MSCP peripheral on the system is identified to the operating system by an MSCP device name. An MSCP device name consists of a device class identifier and a unit number. The device class is indicated by a two-letter prefix; MSCP disk devices are indicated by the prefix DU. Together, the unit number and class prefix form the specification used by the operating system to select a device.

With the exception of MicroVMS systems, DEC operating systems require that all MSCP peripherals on a system have different MSCP device names, even if they are managed by separate MSCP controllers at separate LSI-11 bus device addresses. For example, under RSX-11M-PLUS, if there are three peripherals on the first MSCP controller (at 772150_8), then the first peripheral on the second MSCP controller (in floating CSR address space) is numbered DU3.

3.2.3 PERIPHERAL CAPACITIES

The capacity of peripherals in an MSCP subsystem is measured in logical blocks. Each logical block contains 512 bytes of data. The MSCP controller reports the capacity of a peripheral to the operating system. A 10M byte peripheral such as DEC's RD51 is able to store about 20,000 logical blocks.

3.3 A DEC MSCP SUBSYSTEM

A typical DEC MSCP subsystem for the LSI-11 bus is organized as shown in Figure 3-1. The MSCP host and controller functions are combined in a single piece of hardware, which is referred to as the RQDX1. The hard disk drive that attaches to the RQDX1 is referred to as the RD51, RD52, or RD53 and the 5.25-inch floppy as the RX50. The RQDX1 plugs directly into the LSI-11 bus and is attached to the disk drives via a disk-drive-native interface. These model numbers are not used to identify peripherals to the operating system, but are displayed to the operator by some operating systems during configuration for informational purposes.

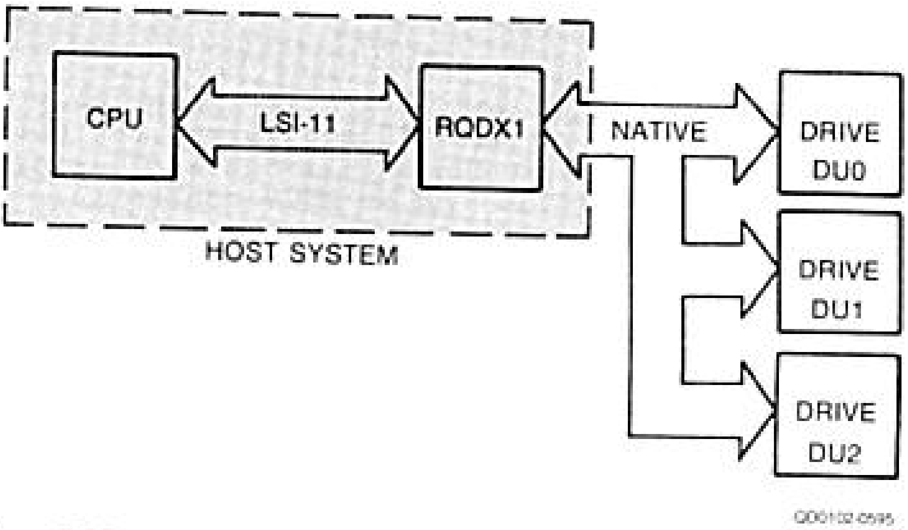

Figure 3-1. DEC MSCP Subsystem Logical and Physical Configuration

3.4 THE QD01/D MSCP SUBSYSTEM

Figure 3-2 illustrates a typical QD01/D MSCP subsystem. As with the DEC implementation, the QD01/D is connected directly to the LSI-11 bus. On the other side the QD01/D uses the ST-506 interface to communicate with one or two disk drives.

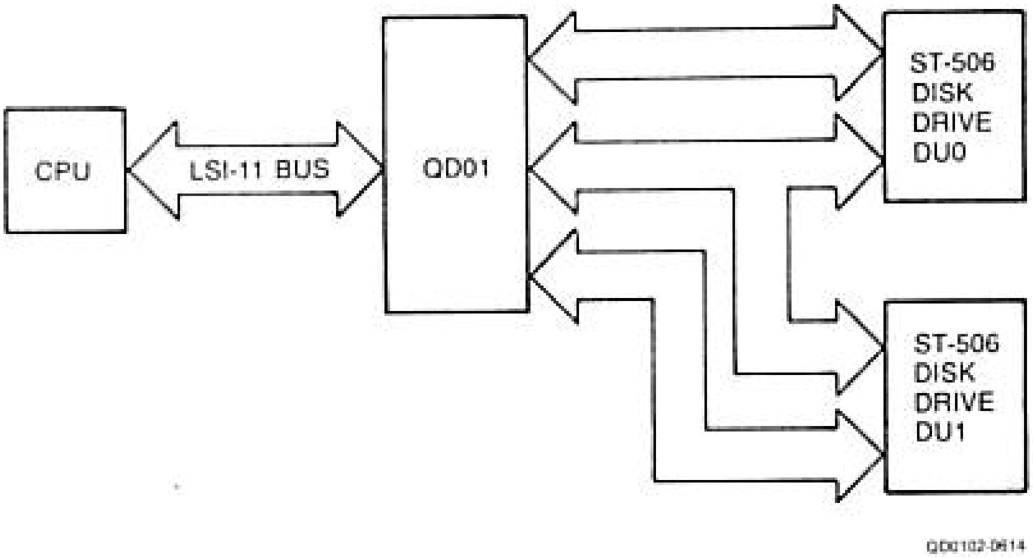

Figure 3-2. QD01/D Subsystem Logical and Physical Configuration

The MSCP subsystem provided by the QD01/D is essentially analogous to the DEC MSCP subsystem. As in the DEC subsystem, the QD01/D MSCP controller connects directly to the LSI-11 bus and performs many of the same functions as the RQDX1. As an MSCP controller, the QD01/D receives requests from the host, optimizes the requests, generates ST-506 commands to perform the operations, transfers data to and from the host, transfers data to and from the device, and buffers data as necessary. When the command is complete, the controller sends a response to the host.

The QD01/D also performs all of the functions of the peripheral controller, including serialization and deserialization of data. The QD01/D connects to the peripherals it supports via the ST-506 interface.

3.4.1 LOGICAL UNIT NUMBERS

As noted in subsection 3.2.2, most DEC operating systems do not allow any MSCP disk devices on one computer to have the same unit number, even though they may be controlled by separate MSCP controllers at different LSI-11 bus addresses.

DEC MSCP-type drives can accept unit identification plugs that define addresses from 0 to 255. ST-506 disk drives and the QD01/D do not have this flexibility; the QD01/D can detect only two unique drive addresses at its ST-506 interface - 0 and 1. To prevent a unit-number conflict between the QD01/D's drives and another MSCP controller's drives, the QD01/D has switches that can be used to change the unit numbers reported to the operating system for its drives.

Example 3-1	An MSCP controller at a standard base address supports four disk drives; a QD01/D at an alternate base address supports two disk drives. An offset of 4 is specified for the QD01/D. This causes the QD01/D disk with address 0 to be reported to the operating system as logical unit number (LUN) 4. The QD01/D disk 1 is reported as LUN 5.

The offset for the logical unit number is specified by using switches SW1-2 through SW1-4 on the QD01/D. See subsection 4.3.3.2.2 for switch setting information.

3.4.2 QD01/D MSCP SUBSYSTEM LOGICAL CONFIGURATION

This subsection explains the algorithm used by the QD01/D to map logical MSCP peripherals onto the physical disk drives provided by the QD01/D subsystem.

3.4.2.1 Logical Devices

The phrase "logical MSCP disk drive" refers to the disk drive as it appears to the operating system. That is, the operating system associates a disk drive of known type (in this case, an MSCP disk drive) with a unit number and a capacity. The QD01/D MSCP controller presents that information to the operating system on command, after initialization.

Because the MSCP controller is responsible for establishing the relationship between unit number and capacity, it is possible for the controller to divide its physical disk drives into more than one logical unit. That is, if a physical disk drive has a capacity of 234,090 blocks, the MSCP controller can divide that capacity into unequal parts: for example, 208,080 blocks and 26,010 blocks. Each part is then assigned a separate unit number, and the the unit number and capacity of each part is presented to the operating system.

The operating system then sees the two parts as separate disk drives, even though the data is actually stored on the same physical drive. The two parts are called logical disk drives, and the numbers that identify them are called MSCP unit numbers.

A drive configuration that supports multiple logical units is specified by the data that is stored in the configuration Nonvolatile Random Access Memory (NOVRAM). Information for programming the configuration NOVRAM is given in Section 6, Registers and Programming. The field that causes a drive to be divided into multiple logical units is called the Split Code (word 11). There are three types of split codes: no split, cylinder split, and head split:

- The use of the first type is obvious. When no split is specified, the entire physical drive is one logical drive.
- Cylinder split codes divide a physical drive by cylinders. The split code specifies a ratio such as half and half, or seven-eighths/one-eighth. The cylinders assigned to a logical drive are contiguous. For example, if the physical drive has 645 cylinders and is split 50/50, the first 322 cylinders are assigned to one drive and the second 322 cylinders are assigned to the other (the odd cylinder is not used).
- Head split codes divide the drive by data heads. A Starting Head Offset field in the NOVRAM specifies the first head of the second logical drive. When the drive is split by data heads, each logical drive has its own platter(s); consequently, the lower blocks of one logical drive are in the same physical cylinder as the lower blocks of the other logical drive. For example, a Maxtor drive, which has fifteen data heads, might be divided so that Drive 0 is assigned heads 0 through 6 and Drive 1 assigned heads 7 though 14. In this example, the Starting Head Offset has a value of 7.

The head splitting technique has a performance advantage over the cylinder method. Typically, most disk accesses are made in the lower cylinders of a disk because many system-oriented files are located there, including the drive's directory. Because the low (and high) cylinders are vertically aligned between the two logical drives when the head splitting technique is used, switching between head-split logical drives requires less head movement than switching between cylinder-split drives.

3.4.2.2 Device Numbers

As with any MSCP subsystem, the drives on the QD01/D are identified using unit numbers. The conventions for numbering multiple MSCP drives vary by operating system.

RSX-11M-PLUS and RT-11 assign MSCP device numbers beginning with zero (DU0). This number is assigned to the first drive on the first MSCP controller, where "first" means the controller located at the standard LSI-11 bus address. Unit number 1 would be the second drive on the first controller, etc. If there are two MSCP controllers on the system, the units installed on the second begin numbering at n+1, where n equals the highest unit number of the first MSCP controller.

RSTS/E requires that drives supported by a standard MSCP controller be numbered starting at 0 and drives supported by an alternate MSCP controller be numbered starting at 4.

Because MSCP device names under MicroVMS designate the supporting MSCP controller, the unit numbering is less restricted. For example, two drives which are supported by a standard MSCP controller might be DUA0 and DUA1 and a third drive supported by an alternate MSCP controller might be DUB0.

Table 3-1 is an MSCP unit numbering example under the RSX-11M operating system that shows the MSCP number versus the actual physical addresses assigned to all the components. The physical disk drive (unit number 0) of the second controller is split into two logical units. Note that two device names are associated with that drive.

Table 3-1. Subsystem Configuration Example

QD01/D Address	Device Description	Drive Unit Number	Device Name
772150	Atasi 3046	0	DU0
	Atasi 3046	1	DU1
760334	Maxtor XT1140 (split 50/50)	0	DU2 DU3
	Maxtor XT1140	1	DU4

NOTE

> All of the MSCP peripherals supported by the QD01/D use the same device identifier - RA81. Unique device identifiers are not available to the host because of the nature of the NOVRAM.

3.5 OPERATING SYSTEMS, DEVICE AND VECTOR ADDRESSES

Before the installation of any peripheral device can be considered complete, the computer's operating system must be made aware of the new resource. The information provided in this section is intended to supplement your DEC operating system resources and to be used as an aid in planning the installation of your QD01/D.

An operating system can be made aware of a new resource in three ways:

- The operating system can poll the computer's I/O device address space.
- The device can be manually connected using CONNECT or CONFIGURE statements.
- The user can tell the operating system about a device during an interactive SYSGEN procedure.

The first technique is referred to as autoconfigure, and it is essentially automatic. The second technique requires that CONNECT statements be placed in a special command file that is executed each time the computer is powered up. The third technique, interactive SYSGEN, creates a configuration file that the operating system references when the system is powered up. All techniques accomplish the same result: they associate a specific device type with a bus address and interrupt vector.

Most recent versions of DEC operating systems use autoconfigure to some extent, and try to follow the same rules. The RT-11 operating system does not use autoconfigure, but can locate devices that reside at a standard address. There are some differences among operating systems, however, especially with regard to MSCP controllers at alternate LSI-11 bus addresses. The following paragraphs address these differences for each supported operating system. This discussion includes information on choosing appropriate LSI-11 bus device addresses and interrupt vectors for the subsystem.

LSI-11 Bus Device Addresses:

The following operating system discussions give procedures for choosing LSI-11 bus addresses for the first MSCP controller and any subsequent controllers in the host configuration. No instructions are provided for programming the chosen address into the QD01/D. See subsection 4.5.1 for detailed switch setting information.

MSCP-type controllers contain two registers that are visible to the LSI-11 bus I/O page. They are the Initialization and Polling (IP) register (base address) and the Status and Address (SA) register (base address plus 2). The IP register, the CSR address, LSI-11 bus address and the base address all refer to the same register. All of the operating systems described in the following subsections use the standard LSI-11 bus address of 772150_8 for the first controller on the host system.

Vector Addresses:

Vector addresses for MSCP controllers are not selected by using switches on the controller PWB, but are programmed into the controller during the Initialization process. Many operating systems select the vector address automatically. If an operating system requires manual input of the vector, the procedure notes that fact.

Device Names:

Again, although DEC has attempted to standardize treatment of peripherals by operating systems, some differences do exist. Table 3-2 lists and describes the device names assigned to MSCP devices under five operating systems. Two controller names and two drive names are given to indicate the numbering scheme.

Table 3-2. Device Names

Operating System	Controller First, Second	Drives Supported by First Controller
RSTS/E	RU0, RU1	DU0, DU1
RSX-11M	---- ----	DU0, DU1
RSX-11M-PLUS	DUA, DUB	DU0, DU1
RT-11	Port0, Port1	DU0, DU1
MicroVMS	PUA, PUB	DUA0, DUA1

Assumptions:

The information regarding operating systems in these subsections is subject to change. The following discussions are based on three assumptions:

- This is the first pass that is being made through SYSGEN; therefore, no saved answer file exists. Answer **N** (no) to questions such as "Use as input saved answer file?"
- Your host system configuration conforms to the standard LSI-11 device configuration algorithm (otherwise autoconfigure results are not reliable).
- You are generating a mapped version of the operating system on the appropriate hardware (unless you are using RT-11).

3.5.1 RSTS/E OPERATING SYSTEMS (V8.0 and above)

RSTS/E scans the hardware to determine configuration each time the system is bootstrapped. The scanning program is called INIT.SYS and it relies on the same hardware configuration conventions as do the other DEC operating systems.

The RSTS/E operating system can support two MSCP controllers. The first MSCP controller must be located at the standard LSI-11 bus address, 772150_8. According to DEC documentation, the second unit should be located in floating address space. For an alternate QD01/D, Emulex suggests specifying a LSI-11 bus address of 760334_8 using the HARDWARE sub-option of the INIT.SYS program.

The INIT.SYS program uses a user-specified table, located in the currently installed monitor, to make exceptions to the autoconfigure algorithm. This table is modified by the HARDWARE option of the INIT.SYS program. Use of this table allows an MSCP controller to be placed at virtually any address on the I/O page. Note that this table must be reset any time a new monitor is installed. Emulex suggests using a LSI-11 bus address of 760334_8 for an alternate QD01/D. An MSCP controller must be located at the standard address to be a bootstrap device.

Interrupt vector addresses are assigned to the MSCP controllers by INIT.SYS and programmed into the devices during initialization.

3.5.2 RT-11 OPERATING SYSTEMS (V5.1 and above)

The RT-11 Operating System supports up to four MSCP controllers with up to 256 devices (total) on the four controllers. The following paragraphs discuss the LSI-11 bus and vector addresses for MSCP controllers under RT-11 in host systems with only one MSCP controller and in those with more than one controller. Disk partitioning, a unique feature of RT-11 that is applicable regardless of the number of controllers, is also discussed.

3.5.2.1 Installing a Single MSCP Controller

If your host system includes only one MSCP controller, install it with a LSI-11 bus address of 772150_8. RT-11 will find and install the handler (driver) for that controller. In single MSCP controller configurations, it is not necessary to run SYSGEN. You may use one of the pregenerated monitors that are provided with the RT-11 Distribution. Emulex recommends that you modify the system start-up command file, STARTx.COM, to properly partition the disk drives. See subsection 3.5.2.3.

3.5.2.2 Installing Multiple MSCP Controllers

If your host system includes more than one MSCP controller, you may either modify the MSCP handler as described in the RT-11 Software Support Manual or perform a SYSGEN. The following procedure describes the SYSGEN technique (user input is in **boldface** print):

1. Initiate SYSGEN:

   IND SYSGEN<return>

   Answer the next group of questions appropriately.

2. Indicate that you want the system to use the start-up command file when booting:

   ```
   Do you want the start-up indirect
   file (Y)? Y<return>
   ```

   The start-up command file is required to allow additional MSCP controller LSI-11 bus addresses to be specified and to partition the disks consistently when the system is bootstrapped. Answer the next set of questions appropriately.

3. Indicate that you want MSCP support when the Disk Options question appears:

   ```
   Enter the device name you want support for
   [dd]: DU<return>
   ```

4. Indicate the number of MSCP controllers on your system in response to this question:

   ```
   How many ports are to be
   supported (1)? 2<return>
   ```

   RT-11 refers to individual MSCP controllers or controllers as ports. Each port has its own LSI-11 bus and vector addresses.

5. Specify support for all other devices in your host system configuration as well. Indicate that there are no more devices by entering a period:

```
Enter the device name you want support for
[dd]: .<return>
```

6. You must specify the addresses of all MSCP controllers (ports) using the SET CSR keyboard command. To ensure that this is done consistently and automatically on power-up, you must add the commands to the system start-up command file, STARTx.COM. The **x** stands for the monitor that is being used, where **x** is S, F, or X for single-job, foreground/background, or extended memory, respectively. Edit the command file to include the following statements:

```
SET DU CSR=772150          (DEFAULT)
SET DU CSR2=760334
SET DU VECTOR=154          (DEFAULT)
SET DU VEC2=300
```

   The LSI-11 bus for the second device can be any unused address in the I/O page which is supported by QD01/D address switch settings; the vector address can be any unused address in the vector page. Default statements are not required.

3.5.2.3 Disk Partitioning

RT-11 is unable to handle drives with a capacity of more than 65,535 blocks (33.5M bytes). To allow drives with larger capacities to be used, RT-11 allows individual physical drives to be partitioned into multiple logical drives. This is done by assigning as many logical drive names (DU0, DU1, etc.) to a physical drive as that drive can support. The statements that make that assignment should be placed in the system start-up command file. This ensures that the drives are automatically partitioned every time the system is bootstrapped and that the partitions are always the same. Use the following procedure to determine the total number of logical drives to be assigned to each physical drive.

1. Determine the drive configuration(s) that you intend to use. You need to know the LUN of each logical drive and the data storage capacity (in logical blocks) of each logical unit. If the QD01/D is at an alternate LSI-11 bus address (not 772150_8), then you must specify an MSCP device number by using switches SW1-2 through SW1-4 (see subsection 4.3.3.2.2).

2. Divide the capacity for each MSCP Unit by 65,535. If the result is a number greater than 1, then that MSCP Unit should be partitioned into multiple logical units. (The last partition on a disk may be smaller that 65,535 blocks.) Round the result up to the nearest whole number. That whole number equals the number of logical disks into which that MSCP unit should be partitioned.

3. You must then include a series of statements in the system start-up command file, STARTx.COM, that assigns logical names to each partition. Each statement has the following format:

   ```
   SET DUn UNIT=y PART=x PORT=z
   ```

   where n is the logical device name, y is the physical MSCP unit number, x is the partition number, and z is the controller number. You must do this for each partition on each drive, including drives that can hold only one partition.

Example: You have selected a drive that has a capacity of 219,283 blocks (unit 0) and a drive that has a capacity of 20,002 blocks (unit 1).

$$\frac{219{,}283}{65{,}535} = 3.35 \text{ (4 logical units)}$$

$$\frac{20{,}002}{65{,}535} = 0.31 \text{ (1 logical unit)}$$

Dividing the unit capacities by 65,535 and rounding the result up to the nearest whole number gives the number of logical units into which each should be partitioned.

You begin assigning logical names to the partitions beginning with DU0. Assign logical names to the partitions on MSCP Unit 0 first. The assignments are made as follows:

```
SET DU0 UNIT=0 PART=0 PORT=0
SET DU1 UNIT=0 PART=1 PORT=0
SET DU2 UNIT=0 PART=2 PORT=0
SET DU3 UNIT=0 PART=3 PORT=0

SET DU4 UNIT=1 PART=0 PORT=0
```

Modify the system start-up command file to include the disk partitioning statements.

3.5.3 RSX-11M OPERATING SYSTEMS (V4.0 and above)

RSX-11M SYSGEN is an interrogative program that allows a complete, running RSX-11M system to be configured for a particular hardware environment. SYSGEN is well documented in the RSX-11M System Generation and Installation Guide, and you are expected to rely primarily on that manual. This explanation is provided only to remove some ambiguities that the installation of the QD01/D may present.

SYSGEN supports autoconfigure, and MSCP controllers are detected by autoconfigure. However, autoconfigure detects only the MSCP controller that is located at the standard LSI-11 bus address. Additional MSCP controllers at alternate addresses must be attached to the operating system manually.

NOTE

> If the QD01/D controls the system disk, you must select 22-bit addressing (SW2-6 ON) even if your system has only 256K bytes of memory.

3.5.3.1 Installing a Single MSCP Controller

If you have only one QD01/D, install it at the standard address (772150_8) and use autoconfigure to connect your peripherals. The procedure given in the RSX-11M System Generation and Configuration Guide is adequate for this purpose.

3.5.3.2 Installing Multiple MSCP Controllers

If you have two MSCP controllers, say an RQDX1 and a QD01/D, you must perform a complete manual initialization. We recommend that the RQDX1 be installed at the standard LSI-11 bus address. Locating the QD01/D at the alternate LSI-11 bus address does not prevent its being used as the system device. Both MSCP controllers are connected to the operating system by using the following procedure.

1. Invoke SYSGEN.

```
> SET /UIC=[200,200]<return>
> @SYSGEN<return>
```

2. To indicate that you want to use autoconfigure, answer **Y** (yes) to the following question:

```
*      Autoconfigure the host system hardware?
       [Y/N]: Y<return>
```

3. To indicate that you do not want to override autoconfigure results, answer **N** (no) to this question:

```
          *       Do you want to override Autoconfigure
                  results? [Y/N]: N<return>
```

   Answer the rest of the questions in the SETUP section appropriately, and continue to the next section, TARGET CONFIGURATION. In TARGET CONFIGURATION, the defaults presented for the first group of questions should be accurate for your system because autoconfigure was requested.

4. In response to the question regarding devices, indicate that you have two MSCP-type controllers:

```
          *       Devices: DU=2<return>
                  Devices: .<return>
```

   This entry supersedes the value of 1 that autoconfigure has determined. Typing a period (.) terminates device input.

   Continue through the next four sections, HOST CONFIGURATION, EXECUTIVE OPTIONS, TERMINAL DRIVER OPTIONS, and SYSTEM OPTIONS, answering questions appropriately.

5. When you reach the PERIPHERAL OPTIONS section, SYSGEN asks you questions that pertain only to the MSCP devices on your system. (Unless you indicated that you wished to override other autoconfigure results when you responded to the Devices question, SYSGEN asks questions on those devices.)

   The first question requests information about the controller's interrupt vector address, LSI-11 bus address, the number of DU-type disk drives (there is no default value for this parameter), the number of command rings, and the number of response rings. The question is asked twice, once for controller 0 and once for controller 1, because we have specified two DU-type controllers. The dialog uses the abbreviation contr to indicate controller.

```
          * DU contr 0 [D:154,172150,,4,4]
          154,172150,3,4,4<return>
```

   The standard vector address for MSCP controllers is 154_8. The vector for a second unit should be allocated from floating vector address space. Any unused vector between 300_8 and 774_8 can be allocated. See Appendix A for a description of DEC's algorithm for assigning floating vectors.

The standard LSI-11 bus address for MSCP controllers is 772150_8. The second unit is located in floating LSI-11 bus address space. See Appendix A for a description of the DEC algorithm for assigning floating addresses.

The number of DU-type disk drives depends on the configuration that you have selected for the QD01/D, or on the number of drives that are attached to a DEC MSCP controller.

When you select a configuration for the QD01/D, you are taking into account the number of physical disk drives that you are attaching to the QD01/D's ST-506 interface. When you select a configuration, you are also specifying a logical arrangement for the QD01/D MSCP subsystem. Some configurations split one physical drive into two logical drives to make file management easier. You determine the configuration of each ST-506 disk drive when you program the QD01/D's NOVRAM; see Section 6.

The following types of disk drives can be attached to DEC MSCP controllers:

- RX50
- RD51
- RD52
- RD53
- RC25
- RA60
- RA80
- RA81

The RX50 drive contains two 5.25-inch floppy diskettes; count an RX50 as two drives. The RC25 drive has both fixed and removable hard media; count an RC25 as two drives.

RSX-11M supports up to eight command and eight response rings; the number of command and response rings that you specify depends on your application. Four command and four response rings are reasonable and adequate for most applications. For further information about command and response rings, refer to the MSCP documentation listed in subsection 6.3 of this manual. In most instances, further information is not required to install the QD01/D.

6. SYSGEN then asks you to specify the type of disk drive(s) on each controller:

   ```
   * DU contr 0 unit 0. is an RA60/80/81/RC25/RD51/RX50
   [D:RA81] RD51<return>
   ```

   For the RQDX1, indicate that you have an RD51 and two RX50 (in that order).

   For the QD01/D, indicate that you have one RD51 for each logical disk drive.

   RSX-11M does not tolerate gaps in sequence; the unit numbers must be contiguous. In addition, the unit numbers specified for each controller must be the same as those reported by the controller during initialization.

3.5.4 RSX-11M-PLUS OPERATING SYSTEMS (V2.1 and above)

RSX-11M-PLUS SYSGEN is an interrogative program that allows a complete, running RSX-11M-PLUS system to be configured for a particular hardware environment. SYSGEN is well documented in the RSX-11M-PLUS System Generation and Installation Guide, and you are expected to rely primarily on that manual. This explanation is provided only to remove some ambiguities that the installation of the QD01/D may involve.

SYSGEN supports autoconfigure, and MSCP controllers are detected by autoconfigure. However, autoconfigure detects only the MSCP controller that is located at the standard LSI-11 bus address. Additional MSCP controllers at alternate addresses must be attached to the operating system manually.

3.5.4.1 Installing a Single MSCP Controller

If you have only one QD01/D, install it at the standard address (772150_8) and use autoconfigure to connect your peripherals. The procedure given in the RSX-11M-PLUS System Generation and Configuration Guide is adequate for this purpose.

3.5.4.2 Installing Multiple MSCP Controllers

If your initial system configuration includes two MSCP controllers, connect the alternate MSCP controller to the operating system during the initial SYSGEN. We recommend that you use autoconfigure to connect the first controller at the standard address (772150_8). We recommend that the RQDX1 be installed at the standard LSI-11 bus address; locating the QD01/D at the alternate LSI-11 bus address does not prevent its being used as the system device.

If you are adding the second MSCP controller to the system configuration, use the Add a Device option of SYSGEN or a complete SYSGEN. The following procedure describes the Add a Device process (user input is in **boldface** print:

1. Invoke SYSGEN.

```
> SET /UIC=[200,200]<return>
> @SYSGEN<return>
```

2. To indicate that you want to do a subset of the SYSGEN procedure, answer **N** (no) to the following questions:

```
* SU120   Do you want to do a complete SYSGEN?
          [Y/N D:Y]: N<return>

* SU130   Do you want to continue a previous SYSGEN
          from some point? [Y/N D:Y]: N<return>
```

3. To indicate that you want to execute a specific module of the SYSGEN procedure, answer **Y** (yes) to this question:

```
* SU150   Do you want to do any individual sections
          of SYSGEN? [Y/N D:Y]: Y<return>
```

4. Select the Add a Device section of SYSGEN:

```
* SU160   Which sections would you like to do?
          [S R:0.-15.]: H<return>
```

   Type the letter H to select the Add a Device section. SYSGEN now asks you all of the questions in the Choosing Peripheral Configuration section.

   The questions that SYSGEN asks pertain to the type and number of controllers that are installed on your system. There is one question for each type of controller that RSX-11M-PLUS can support. Answer 0 (zero) for all types of controllers until you are prompted for the number of UDA-type devices.

5. When you are asked to specify the number of MSCP-type devices, answer appropriately:

```
* CP3004  How many MSCP disk controllers do you
          have? [D R:0.-63. D:0.] 2<return>
```

6. Give the total number of MSCP disk drive (on all controllers) installed on the system.

```
    * CP3008  How many MSCP disk drives do you have?
              [D R:0.-n. D:1.] 5<return>
```

The answer to this question depends on the configuration that you have selected for the QD01/D and on the number of drives that are attached to any DEC MSCP controllers.

When you select a configuration for the QD01/D, you are taking into account the number of physical disk drives that you are attaching to the QD01/D's ST-506 interface. When you select a configuration, you are also specifying a logical arrangement for the QD01/D MSCP subsystem. Some configurations split one physical drive into two logical drives to make file management easier. You determine the configuration of each ST-506 disk drive when you program the QD01/D's NOVRAM (see Section 6).

The following types of disk drives can be attached to DEC MSCP controllers:

- RX50
- RD51
- RD52
- RD53
- RC25
- RA60
- RA80
- RA81

The RX50 drive contains two 5.25-inch floppy diskettes; count an RX50 as two drives. The RC25 drive has both fixed and removable hard media; count an RC25 as two drives.

7. SYSGEN then asks you to specify controllers per disk drives.

```
    * CP3044  To which DU controller is DU0: connected?
              [S R:1-1]: A<return>
```

This question is asked as many times as the number of MSCP drives that you have indicated are on the system. RSX-11M-PLUS does not tolerate gaps in sequence; the MSCP unit numbers must be contiguous. In addition, the unit numbers specified for each controller must be the same as those reported by the controller during initialization. Use A for the primary controller and B for the alternate controller.

8. Enter the vector address for each MSCP controller:

```
        * CP3068  Enter the vector address of DUA
                  [O R:60-774 D:154]
```

The standard vector address for MSCP controllers is 154_8. The vector for a second unit should be allocated from floating vector address space. Any unused vector between 300_8 and 774_8 can be allocated. See Appendix A for a description of DEC's algorithm for assigning floating vectors.

9. Enter the CSR address for each MSCP controller:

```
        * CP3072  What is its CSR address?
                  [O R:160000-177700 D:172150]
```

The standard CSR address for MSCP controllers is 772150_8. The second unit can be located in floating CSR address space. See Appendix A for a description of the DEC algorithm for assigning floating addresses.

10. Specify the number of command rings for each MSCP controller:

```
        * CP3076  Enter the number of command rings for DUA
                  [D R:1.-8. D:4.] 4<return>
```

RSX-11M-PLUS supports up to eight command rings. The value you specify depends on your application. Four command rings are reasonable and adequate for most applications. For further information about command and response rings, refer to the MSCP documentation listed in subsection 6.3 of this manual. In most instances, further information is not required to install the QD01/D.

10. Specify the number of response rings for each MSCP controller:

```
        * CP3076  Enter the number of response rings for DUA
                  [D R:1.-8. D:4.] 4<return>
```

RSX-11M-PLUS supports up to eight response rings. The value you specify depends on your application. Four response rings are reasonable and adequate for most applications.

3.5.5 MicroVMS OPERATING SYSTEMS

MicroVAX/MicroVMS supports MSCP controllers at the standard address, 772150_8, and in floating address space. MicroVMS has a software utility called SYSGEN which can be used to determine the LSI-11 bus address and interrupt vector address for any I/O devices to be installed on the computer's LSI-11 bus. A running MicroVAX/MicroVMS computer system is required in order to use this utility.

If you do not have access to a running system, you must determine the LSI-11 bus addresses and vector addresses manually (although autoconfigure can still be used to connect the devices to the computer automatically on power-up). See Appendix A for a description of the algorithm used by SYSGEN to determine LSI-11 bus addresses.

NOTE

> If you are installing a second MSCP controller in a MicroVAX system which includes a DZV11 controller, you must locate the second MSCP device at 760354_8.

The following procedure tells how to use MicroVMS SYSGEN to determine LSI-11 bus addresses and interrupt vectors.

1. Login to the system manager's account (this procedure requires system manager privileges). Run the SYSGEN utility:

   ```
   $ RUN SYS$SYSTEM:SYSGEN<return>
   SYSGEN>
   ```

   The SYSGEN> prompt indicates that the utility is ready to accept commands.

2. Obtain a list of devices already installed on the MicroVAX LSI-11 bus by typing:

   ```
   SYSGEN> SHOW/CONFIGURATION<return>
   ```

```
Name: PUA  Units: 1  Nexus: 0  CSR: 772150   Vector1: 154  Vector2: 000
Name: TXA  Units: 1  Nexus: 0  CSR: 760500*  Vector1: 310* Vector2: 000

*Floating address or vector
Note: All addresses and vectors are expressed in octal notation.
```

Figure 3-3. Sample SHOW CONFIGURATION

SYSGEN lists by logical name the devices already installed on the LSI-11 bus. Make a note of these other devices with floating addresses (greater than 760000_8) or floating vectors (greater than 300_8) that you plan to re-install with your QD01/D.

3. To determine the LSI-11 bus addresses and vectors that autoconfigure expects for a particular device type, execute the CONFIGURE command:

   ```
   SYSGEN> CONFIGURE<return>
   DEVICE>
   ```

   Specify the LSI-11 bus devices to be installed by typing their LSI-11 bus names at the DEVICE prompt (the device name for MSCP controllers under MicroVMS is UDA).

   ```
   DEVICE> UDA,2<return>
   DEVICE> DHV11<return>
   ```

   A comma separates the device name from the number of devices of that type to be installed. The number of devices is specified in decimal.

   In addition to the QD01/D, you need only specify devices that have floating addresses or vectors. Devices with fixed addresses or vectors do not affect the address or vector assignments of devices with floating addresses and vectors.

4. Indicate that all devices have been entered by pressing the <ctrl> and Z keys simultaneously:

   ```
   DEVICE> ^Z
   ```

   SYSGEN lists the addresses and vectors of the devices entered in the format shown in Figure 3-4.

```
SYSGEN>  CONFIGURE
DEVICE> DHV11
DEVICE> UDA,2
DEVICE> ^Z
Device: UDA     Name: PUA   CSR: 772150    Vector: 154    Support: yes
Device: UDA     Name: PUB   CSR: 760334*   Vector: 300*   Support: yes
Device: DHV11   Name: TXA   CSR: 760500*   Vector: 310*   Support: yes

*Floating address or vector
Note: All addresses and vectors are expressed in octal notation.
```

Figure 3-4. CONFIGURE Command Listing

5. Note the CSR addresses listed for the LSI-11 bus devices in floating address space. Program the listed addresses into non-Emulex devices as instructed by the manufacturer's documentation. For the QD01/D, program the address given for the QD01/D (lowest numerical address) into the board as described in subsection 4.3.1.

If you want to select a non-standard address for the QD01/D, that is one that differs from the address selected by the CONFIGURE command, you must enter CONNECT statements in the SYSCONFIG.COM file that is in the system manager's account, SYS$MANAGER. Use the syntax of the CONNECT statements as described in the DEC documentation on MicroVMS SYSGEN.

NOTE

> Do not alter the STARTUP.COM or UVSTARTUP.COM command files in the main system account, SYS$SYSTEM.

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Section 4
INSTALLATION

4.1 OVERVIEW

The procedure for installing the QD01/D Disk Controller is described in this section. The subsection titles are listed below to serve as an outline of the procedure.

Subsection	Title
4.1	Overview
4.2	Inspection
4.3	Disk Controller Setup
4.4	Physical Installation
4.5	ST-506 Disk Drive Preparation
4.6	Cabling
4.7	Integration and Operation

If you are unfamiliar with the subsystem installation procedure, Emulex recommends reading this Installation Section before beginning.

4.1.1 SUBSYSTEM CONFIGURATIONS

This section is limited to switch setting data and physical installation instructions. No attempt is made to describe the many subsystem configurations that are possible. **If you are not familiar with the possible configurations, we strongly recommend reading Section 3, PREPARING THE INSTALLATION, before attempting to install this subsystem.**

When you are installing the subsystem, you should make a record of the subsystem configuration and environment. Figure 4-1 is a Configuration Record Sheet that lists the information required and shows where the data can be found. This information will be of help to an Emulex service representative should your subsystem require service.

QD01/D CONFIGURATION REFERENCE SHEET

GENERAL INFORMATION

- Host computer type ________________
- Host computer operating system ________________
  Version ________________
- Other MSCP Controllers; Type ________________ , LSI-11 Bus Address ________________

DRIVE CONFIGURATION PARAMETERS

- Drive Manufacturer (0) ________________ Model ________________
- Drive Manufacturer (1) ________________ Model ________________
- NOVRAM Paramenters:

DRIVE 0

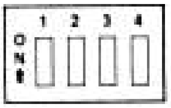
0	Number Units	______
1	Type Code	______
2	Head Offset	______
3	Sectors/Track	______
4	Heads	______
5	Cylinders	______
6	Spare Sectors	______
7	Alternate Cylinders	______
10	Reserved	______
11	Split Code	______
12	Removable Media	______
13	Hard/Soft Sector	______
14	Reduced Write	______
15	Write Precomp.	______
16	Step Code	______
17	Spiral Offset	______

DRIVE 1

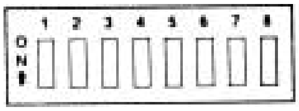
0	Number Units	______
1	Type Code	______
2	Head Offset	______
3	Sectors/Track	______
4	Heads	______
5	Cylinders	______
6	Spare Sectors	______
7	Alternate Cylinders	______
10	Reserved	______
11	Split Code	______
12	Removable Media	______
13	Hard/Soft Sector	______
14	Reduced Write	______
15	Write Precomp.	______
16	Step Code	______
17	Spiral Offset	______

QD01/D CONFIGURATION

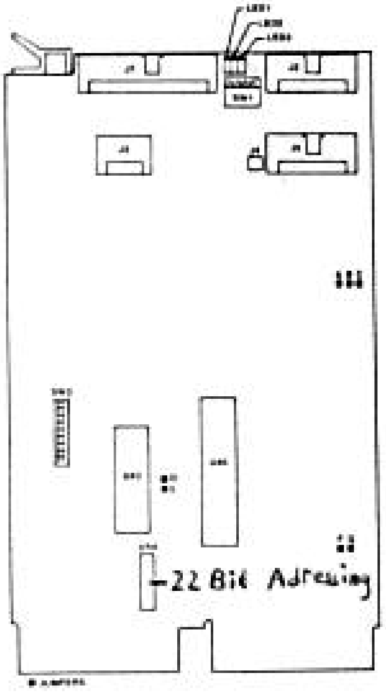
- Firmware revision number ________________
- Top assembly number ________________
- LSI-11 Bus address ________________
- Warranty expiration date ________________
- Serial number ________________
- Interrupt vector address ________________
- 22-bit addressing IC (AMD 7438) installed (Y or N) ________________
- Switch settings (☐ = OFF ■ = ON)



SW1



SW2



Use Pencil

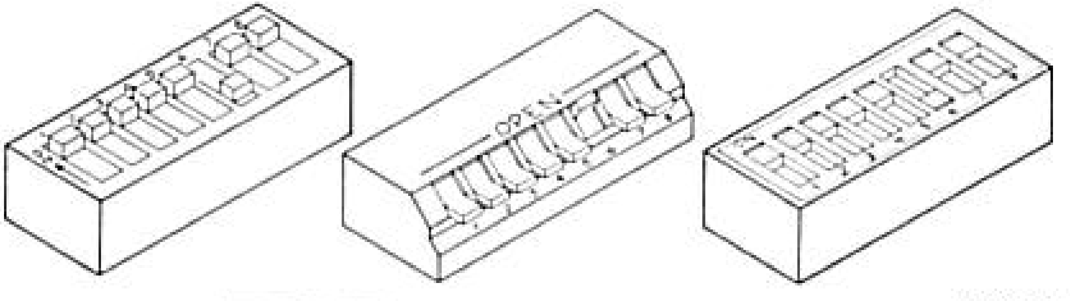
QD0102-0685

Figure 4-1. QD01/D Configuration Reference Sheet

4.1.2 DIP SWITCH TYPES

Switch-setting tables in this manual use the numeral one (1) to indicate the ON (closed) position and the numeral zero (0) to indicate the OFF (open) position.

The three DIP switch types used in this product are shown in Figure 4-2. Each is set to the code shown in the switch setting example.



SW1							
1	2	3	4	5	6	7	8
1	1	1	1	1	0	1	1

Figure 4-2. Switch Setting Example

4.1.3 MAINTAINING FCC CLASS A COMPLIANCE

Emulex has tested the QD01/D Intelligent Disk Controller with DEC computers that comply with FCC Class A limits for radiated and conducted interference. When properly installed, the QD01/D does not cause compliant computers to exceed Class A limits.

There are two possible configurations in which the QD01/D and its associated ST-506 peripherals can be installed:

- With both the QD01/D Disk Controller and the ST-506 disk drives both mounted in the same cabinet, and
- With the QD01/D mounted in the CPU cabinet and the ST-506 drives mounted in a separate cabinet.

To limit radiated interference, DEC completely encloses the components of its computers that generate or could conduct radio-frequency interference (RFI) with a grounded metal shield (earth ground). During installation of the QD01/D, nothing must be done that would reduce this shield's effectiveness. That is, when the QD01/D installation is complete, no gap in the shield that would allow RFI to escape can be allowed.

Conducted interference is generally prevented by installing a filter in the AC line between the computer and the AC outlet. Most power distribution panels that are of current manufacture contain suitable filters.

The steps that must be taken to maintain the integrity of the shield and to limit conducted interference are explained fully in subsection 4.6.

4.2 INSPECTION

Emulex products are shipped in special containers designed to provide full protection under normal transit conditions. Immediately upon receipt, the shipping container should be inspected for evidence of possible damage incurred in transit. Any obvious damage to the container, or indications of actual or probable equipment damage, should be reported to the carrier company in accordance with instructions on the form included in the container.

Unpack the QD01/D subsystem and, using the shipping invoice, verify that all equipment is present. Verify also that model or part numbers (P/N), revision levels, and serial numbers agree with those on the shipping invoice. Paragraph 1.4 explains model numbers and details kit contents. These verifications are important to confirm warranty. If evidence of physical damage or identity mismatch is found, notify an Emulex representative immediately. If the equipment must be returned to Emulex, it should be shipped in the original container.

4.2.1 QD01/D DISK CONTROLLER INSPECTION

Visually inspect the QD01/D Disk Controller after unpacking. Check for such items as bent or broken connector pins, damaged components, or any other evidence of physical damage.

Examine all socketed components carefully to ensure that they are properly seated.

4.3 DISK CONTROLLER SETUP

Several configuration setups must be made on the QD01/D Disk Controller before inserting it into the chassis. These setups are made by option switches SW1 and SW2.

Figure 4-3 shows the locations of the configuration switches referenced in the following paragraphs.

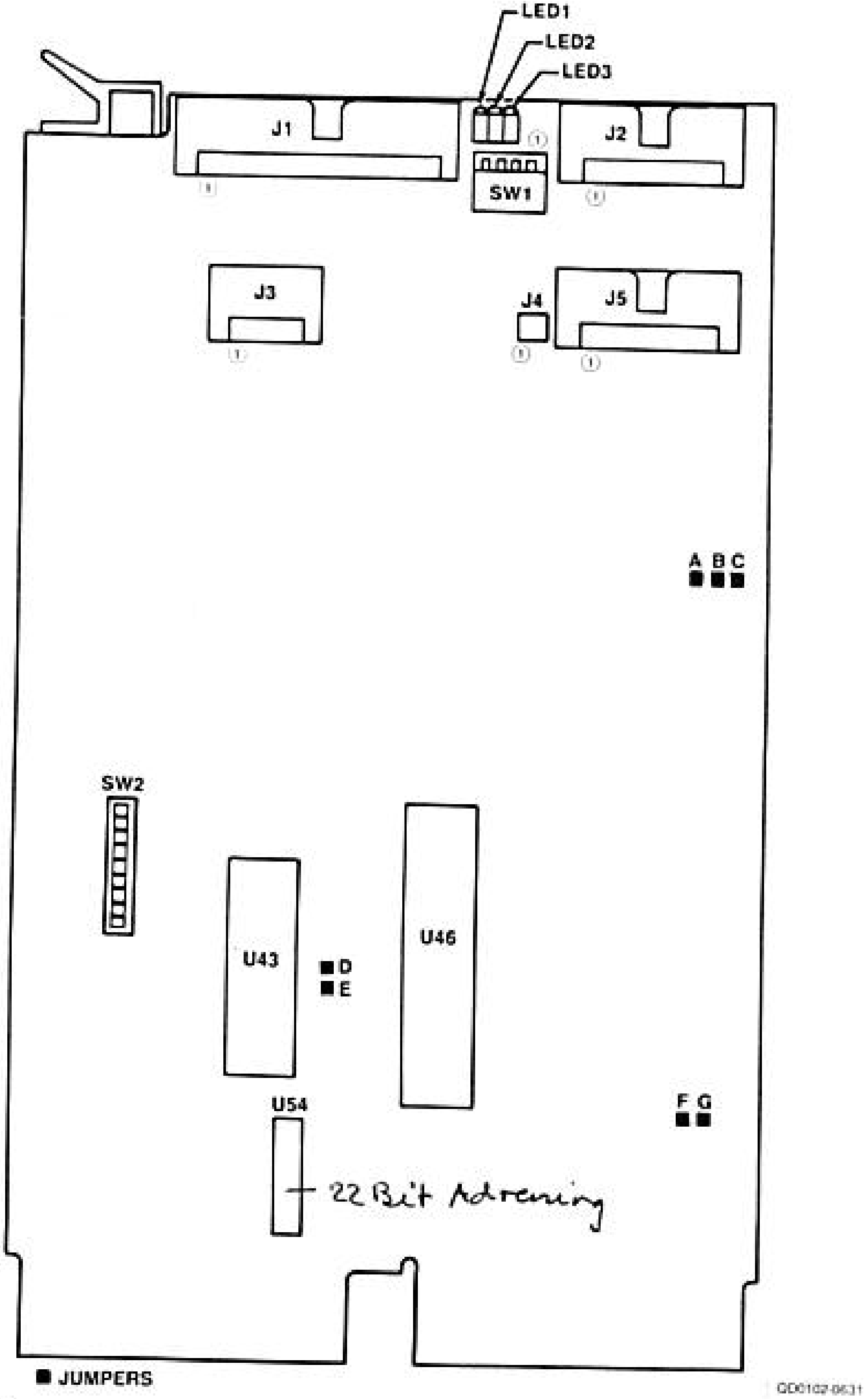


Figure 4-3. QD01/D Disk Controller Assembly

NOTE

> If you change a switch position on the QD01/D, you must also reset the QD01/D so that the host operating system's initialization sequence reads the codes established by the switch settings. To reset the QD01/D, either toggle switch SW1-1 (ON then OFF), or power-down and power-up the the system.

Table 4-1 defines the function and factory configuration of all switches on the QD01/D controller. The factory configuration switch settings are representative of most QD01/D Disk Controller applications.

Table 4-1. QD01/D Switch Definitions and Factory Configuration

SW	OFF(0)	ON(1)	Fact	Function	Section
SW1-1	Run	Reset/Halt	OFF(0)	Run vs. Reset/Halt	
SW1-2	-	-	OFF(0)	MSCP Device Number (LSB)	4.3.3.2
SW1-3	-	-	OFF(0)	MSCP Device Number	4.3.3.2
SW1-4	-	-	OFF(0)	MSCP Device Number (MSB)	4.3.3.2
SW2-1	Disable	Enable	OFF(0)	Loop on Self-test Error	
SW2-2	Disable	Enable	OFF(0)	Automatic Bootstrap	4.3.3.1
SW2-3	-	-	OFF(0)	LSI-11 Bus Address	4.3.1
SW2-4	-	-	OFF(0)	LSI-11 Bus Address	4.3.1
SW2-5	-	-	OFF(0)	LSI-11 Bus Address	4.3.1
SW2-6	18-bit	22-bit	OFF(0)	Twenty-Two-Bit Addressing	4.3.3.3
SW2-7	4 usec	8 usec	OFF(0)	DMA Burst Delay	4.3.3.4
SW2-8	-	-	OFF(0)	Reserved	

ON(1) = Closed
OFF(0) = Open
NS = No standard
Fact = Factory switch setting

Jumpers on the QD01/D are defined as follows:

Jumper	OUT	IN	FACT
A-B	Disable Clock	Enable Clock	IN
C	Not Used	Not Used	OUT
D-E	Not Used	Not Used	OUT
F-G	Normal Operation	Factory Test	OUT

4.3.1 DISK CONTROLLER BUS ADDRESS

Every LSI-11 bus I/O device has a block of several registers through which the system can command and monitor that device. The registers are addressed sequentially from a starting address assigned to that controller, in this case an MSCP-class Disk Controller.

The address for the first of the QD01/D's two LSI-11 bus registers is selected by DIP switches SW2-3 through SW2-5. See Table 4-2 for register address switch settings. For more information on determining the LSI-11 bus address, see Section 3 and Appendix A.

Table 4-2. Controller Address Switch Settings

Bus Address (in octal)	-- SW2 --			Factory
	3	4	5	
772150	0	0	0	√
772154	1	0	0	
760334	0	1	0	
760340	1	1	0	
760344	0	0	1	
760350	1	0	1	
760354	0	1	1	
760360	1	1	1	

4.3.2 INTERRUPT VECTOR ADDRESS

The interrupt vector address for the QD01/D is programmed into the device by the operating system during power-up. See subsection 3.5 for a discussion of vector addresses.

4.3.3 OPTIONS

There are other QD01/D options that can be implemented by the user. These features are selected by physically installing the option on the PCBA or by enabling the option using a switch.

4.3.3.1 Autoboot

The Autoboot option causes the system to boot automatically from logical unit 0 through 3 on power-up when the QD01/D is at the standard bus address. To enable this option, set SW2-1 ON (1). This option cannot be enabled with a MicroVAX or in a system that uses an 11/73B CPU module.

Switch	OFF	ON	Factory
SW2-1	Disable	Enable	OFF

The Autoboot process requires that the LSI-11 CPU be configured for power-up mode 0. The following table lists the configuration settings for several popular LSI-11 CPUs.

CPU	Configuration Setting
11/73A	Install W3 and W7
11/23+	Remove J18-J19 and J18-J17
11/23	Remove W5 and W6
11/02	Remove W5 and W6

If the bootstrap device is not powered-up or safe (e.g., it failed its self-test), the autoboot routine in the QD01/D halts the CPU after one minute. This causes the CPU to enter Console ODT. You can then examine the Status and Address (SA) register (base address plus 2) for a MSCP error code and bootstrap the system from another device.

4.3.3.2 MSCP Device Number

QD01/D switches SW1-2 through SW1-4 specify MSCP device numbers. The functions of these switches are dependent on the options you select for your QD01/D:

- If the QD01/D is installed at the standard LSI-11 bus address, these switches identify the MSCP device number of the drive from which to bootstrap. The QD01/D automatic bootstrap option supports only MSCP units 0 through 3 at the standard address.
- If the QD01/D is installed at an alternate LSI-11 bus address, these switches identify the MSCP device number of the first drive supported by that alternate QD01/D. The first drive supported by the QD01/D at alternate address may be drive 1 through 8.

4.3.3.2.1 Logical Unit to Autoboot From

If the QD01/D automatic bootstrapping option is enabled (SW2-2 ON) and the QD01/D is at the standard LSI-11 bus address (772150_8), switches SW1-2 through SW1-4 define the MSCP device number of the drive from which the QD01/D bootstraps. By using these switches, you may select one of four logical units to bootstrap from. Table 4-3 defines the MSCP device numbers selected by switches SW1-2 through SW1-4 if the QD01/D is at a standard address.

Table 4-3. Bootstrap MSCP Device Number

Bootstrap MSCP Device Number	-- SW1 -- 2	3	4	Factory
0	0	0	0	√
1	1	0	0	
2	0	1	0	
3	1	1	0	

4.3.3.2.2 First Logical Unit Number for an Alternate QD01/D

If your QD01/D is installed at an alternate address, switches SW1-2 through SW1-4 select the MSCP device number of the first drive supported by the QD01/D. MSCP device numbering schemes may vary by DEC operating system (see subsection 3.4.2.2). Table 4-4 defines the MSCP device numbers selected by switches SW1-2 through SW1-4 if the QD01/D is at an alternate address.

Example 4-1: Your system operates under RSX-11M, and has two QD01/D Disk Controllers. The first QD01/D is at the standard LSI-11 bus address for MSCP controllers, 772150_8, and it supports three logical drives, Unit 0, Unit 1, and Unit 2. The second QD01/D is at the alternate LSI-11 bus address, and it supports two logical drives. RSV-11M-PLUS requires that the first drive on the alternate QD01/D have an MSCP device number of 3 and that the second drive have an MSCP device number of 4. Set SW1-2 ON (0), SW1-3 ON (1), and SW1-4 OFF (0) on the alternate QD01/D to specify a MSCP device number of 3 for the first drive.

This example would also apply if the first MSCP controller were a DEC RQDX1 with three logical drives.

Table 4-4. MSCP Device Number for the First Drive on a QD01/D at an Alternate Address

Starting MSCP Device Number	-- SW1 -- 2	3	4
1	1	0	0
2	0	1	0
3	1	1	0
4	0	0	1
5	1	0	1
6	0	1	1
7	1	1	1
8	0	0	0

4.3.3.3 22-Bit Memory Addressing

Twenty-two-bit addressing capability is a standard option for the QD01/D. The QD01/D 22-Bit Addressing Kit, part number QD0113002, is supplied with the QD01/D. To enable 22-bit addressing, install the single AMD7438 IC in socket U154 on the QD01/D PCBA and set SW2-6 ON (1).

CAUTION

Some manufacturers of LSI-11 bus backplanes use the backplane lines now devoted to extended addressing for power distribution. Installing an QD01/D with the extended addressing option in such a system **will** damage the option IC. Before installing the option, confirm that there is neither positive nor negative potential between lines BC1, BD1, BE1, BF1, and logic ground. An QD01/D without the addressing option will not be damaged if power is present on those lines.

4.3.3.4 DMA Burst Delay

The QD01/D firmware design includes a switch-selectable DMA burst delay to avoid data late conditions. Switch 2-7 selects either a 4-microsecond or 8-microsecond delay between DMA bursts. Even with the QD01/D adaptive DMA, some applications may require a longer burst delay to allow other devices adequate time on the bus.

Switch	OFF	ON	Factory
SW2-7	4 usec	8 usec	OFF

4.4 PHYSICAL INSTALLATION

4.4.1 SYSTEM PREPARATION

To prepare your CPU to accept the QD01/D, use the following procedures:

MICRO/PDP/VAX Preparation:

1. Power down the system by switching OFF the main AC breaker.
2. Remove the rear cover from the chassis so that the patch panel is exposed. The rear cover is held on by snap pads. Grasp the cover at the top and bottom, and pull straight back.
3. Loosen the captive screws from the patch panel using a standard screwdriver.
4. Remove the patch panel.
5. Find the flat-ribbon cable that connects the CPU module to the patch panel. For easier board installation, you may disconnect the CPU flat-ribbon cable from the patch panel.

LSI-11 Series Preparation:

1. Power down the system by switching OFF the main AC breaker.
2. Remove the cover from the chassis so that the backplane is exposed.

Do not replace the covers or patch panels until the installation is verified (subsection 4.7).

4.4.2 SLOT SELECTION

The QD01/D may be assigned to any desired slot because it uses the LSI four-level interrupt scheme to perform distributed interrupt arbitration.

Be sure to find out whether your backplane is straight or serpentine and choose a slot accordingly. On straight backplanes, the QD01/D must be plugged into connectors A and B, since connectors C and D carry no signals. On a serpentine backplane, the QD01/D can be plugged into either connectors A and B or connectors C and D.

There must be no unused slots, however, between the CPU and the QD01/D. If you have a DEC RQDX1 in your backplane, be sure to install the QD01/D in front of the RQDX1; not all RQDX1 controllers pass Nonprocessor Grant (NPG) signals.

4.4.3 MOUNTING

The QD01/D Disk Controller PWB should be plugged into the LSI-11 backplane with components oriented in the same direction as the CPU and other modules. Always insert and remove the boards with the computer power OFF to avoid possible damage to the circuitry. Be sure that the board is properly positioned in the throat of the board guides before attempting to seat the board by means of the extractor handle.

4.5 ST-506 DISK DRIVE PREPARATION

There is only one configuration setup that needs to be made on common ST-506 disk drives: drive unit numbering.

Most ST-506 peripherals must have unit numbers assigned to them during installation. The QD01/D supports drive unit numbers of only 0 and 1. Check the manual supplied with the drive for instructions on how to set the unit drive number.

Select either 0 or 1 for your drives in accordance with the configuration that you have programmed into the NOVRAM. See Section 6, Registers and Programming.

4.6 CABLING

The QD01/D Disk Controller controls its two physical disk drives via a standard ST-506 interface. The interface has two parts: a 34-line control segment, which is connected to both drives, and two 20-line data segments, one of which goes to each drive. The physical interface is implemented by using three headers (J1, J2, and J5) that are located on the outside edge of the PWB. J1 is the control segment header; J2 and J5 are the data segment headers. The control cable that begins at J1 is daisy-chained between the two disk drives, and each of the data cables that begin at J2 and J5 goes to one of the drives. Maximum cable length is 20 ft (6 m).

Table 4-5 lists cables offered by Emulex for the QD01/D. Table 4-6 lists the components that are required to construct both control and data cables. Figure 4-4 shows basic cable installation.

In addition, Emulex offers the QD01 Cabling Kit (P/N QD0113003) for installation in a MICRO/PDP or MicroVAX I or II Tower. The QD01 Cabling Kit, which includes cables and panels for separate cabinet installation, is documented in the QD01 Cabling Kit Instruction Sheet (P/N QD0152401).

Table 4-5. Emulex QD01/D Cables

Cable Description	Part Number	Cable Length
Control, 34-line	QU0111201-01 QU0111201-02 QU0111201-03 QU0111201-04 QU0111201-05 QU0111201-06	3 ft 6 ft 9 ft 12 ft 15 ft 18 ft
Data, 20-line	QU0111202-01 QU0111202-02 QU0111202-03 QU0111202-04 QU0111202-05 QU0111202-06	3 ft 6 ft 9 ft 12 ft 15 ft 18 ft
Daisy-chain, 34-line	QU0111203-01 QU0111203-02 QU0111203-03 QU0111203-04	1 ft 2 ft 3 ft 4 ft

Table 4-6. Interface and Cable Components

Cnctr Number	Controller Function	Header Type	Cable Components			
			Control Cnctr	Cable Type Unshield	Shielded	Drive Cnctr
J1	Control	3594	3414	3801/34	3517/34	3463
J2/J3	Data	3592	3421	3801/20	3517/20	3461

Cnctr = Connector
All component numbers are 3M. Equivalents may be used.

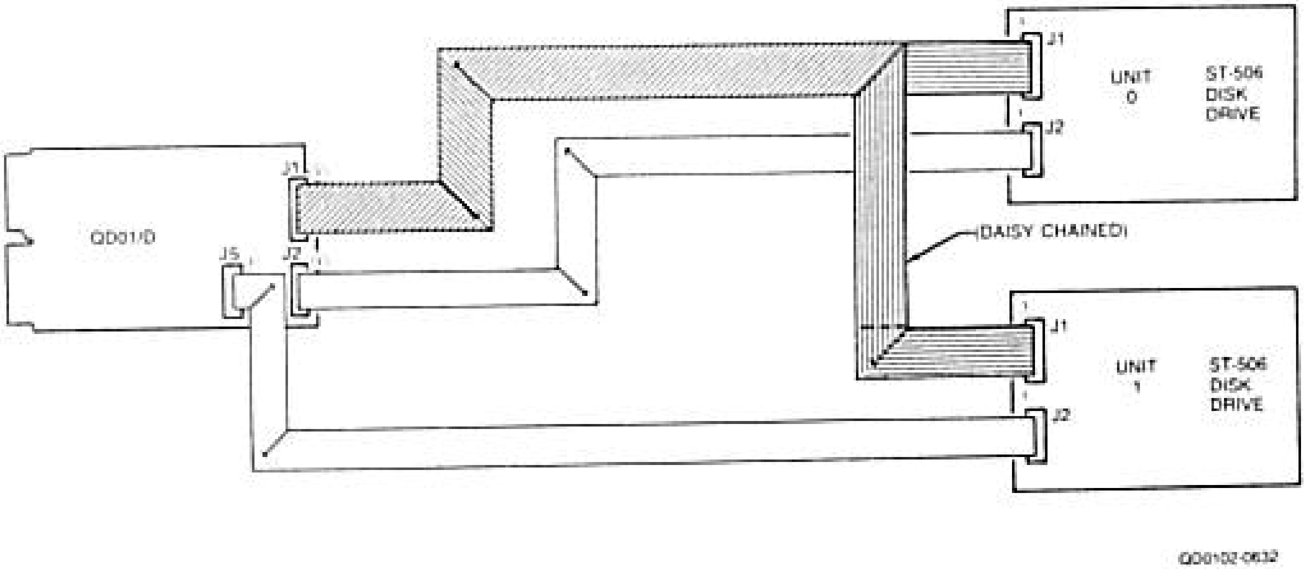


Figure 4-4. QD01/D Cabling Diagram

The Federal Communications Commission (FCC) has mandated that equipment that uses radio-frequency signals in its operation must limit the amount of electromagnetic interference (EMI) that it radiates. Most manufacturers, including DEC, limit EMI by building continuous metal shields into their equipment cabinets.

When installing the QD01/D and its disk drives, you must take care that the shield that DEC has built into its equipment cabinets is not defeated.

The routing of the cables that connect the QD01/D and its disk drives can have a major impact on the amount of EMI that is radiated by the subsystem (the combination of the QD01/D and its drives), especially if the QD01/D and the disk drives are installed in separate cabinets.

As noted in subsection 4.1.3, the QD01/D and its ST-506 disk drive(s) can be installed in either of two configurations:

- With both the QD01/D Disk Controller and the ST-506 disk drive(s) that it supports mounted in the same cabinet
- With the QD01/D mounted in the CPU cabinet and the ST-506 disk drive(s) mounted in a separate cabinet

When the QD01/D and the ST-506 disk drive are installed in the same cabinet, it is possible that the cabinet itself provides sufficient shielding. In such cases, it is not usually necessary to shield the cable that carries the ST-506 interface between the QD01/D and the ST-506 peripherals.

NOTE

> If the cabinet in which the QD01/D and LSI-11 CPU are installed was manufactured before 1 October 1983, it may not provide sufficient shielding or filtering to prevent excessive RFI radiation or conduction. In case of complaint, it is the operator's responsibility to take whatever steps are necessary to correct the interference.

If the ST-506 disk drives are mounted in a separate cabinet from the QD01/D Disk Controller, then the cables that connect the QD01/D to the drives should probably be shielded, because they run outside the shielded cabinet environment.

In addition, you should take special care that the integrity of the shield is maintained where the cables pass though it. Usually, designers use clamps that effectively connect the cable shielding to the cabinet shield.

4.7 INTEGRATION AND OPERATION

Before you can use the QD01/D, you must load the NOVRAM with the configuration parameters of the drives that are controlled by the QD01/D. This can be done in two ways: by using a console emulator or by using a software program. Subsection 6.3.1.1 describes the console emulator technique. The Emulex PDP/LSI MSCP Formatter Program (SXMX8A) and the MicroVAX QD01/D MSCP Disk Formatter Program (FQD01M) are supplied on several Emulex diagnostic program distributions as listed and described in Appendix C.

NOTE

> Drive configuration parameters must be loaded into the NOVRAM before the controller can be used. The NOVRAM is not loaded at the factory, and its contents are indeterminate as delivered by the factory.

4.7.1 DRIVE FORMATTING

Before data can be stored on the QD01/D's disk drives, the drives must be formatted. The same program that Emulex provides to load the QD01/D's drive configuration NOVRAM can also format the disk drives, verify the disk media, and reassign the blocks that it finds to be bad. The QD01/D implements a format option that allows it to format its disk drives without help from system software; however, the QD01/D does not verify the disk media or reassign bad blocks. See subsection 6.3.1.2. We strongly recommend using the Emulex software programs to format and verify the disk media. See subsection 1.4 for ordering information.

4.7.2 TESTING

Successfully loading the NOVRAM and formatting the disk drives gives good indication that the QD01/D and its disk drives are in good operating condition. Figure 5-1 illustrates the loading and formatting procedure in flow chart format, and the figure gives fault isolation information that can be used with the procedure. The Emulex PDP/LSI MSCP Formatter Program (SXMX8A) program follows a similar path, and the fault isolation information can be used with the program as well.

4.7.3 OPERATION

There are no operational instructions. The QD01/D is ready for MSCP initialization as soon as it is powered up.

4.7.3.1 Indicators

There are three light emitting diodes (LED) on the QD01/D PWB. These LEDs are used for both diagnostics and for normal operations.

If switch SW2-1 is OFF, the QD01/D executes a self-test at the following times:

- on power-up
- after a reset condition
- after a bus initialization
- after a write operation to the Initialization and Polling (IP) register (base address)

The self-test routine consists of two test sequences: preliminary and self-test. The preliminary test sequence exercises the 8031 microprocessor chip and the Disk Formatter chip. When the QD01/D successfully completes the preliminary test, LED3 illuminates indicating that the QD01/D is waiting for the MSCP initialization sequence.

During the MSCP initialization sequence, initiated by host software control, the QD01/D executes a second self-test that exercises the buffer controller chip, the Host Adapter Controller (HAC) chip and its associated circuitry, the on-board RAM, and the control memory PROM. If the QD01/D passes this sequences of its self-test successfully, all the LED indicators on the edge of the QD01/D are OFF.

If a fatal error is detected either during self-test or while the system is running, all three of the edge-mounted LED indicators are ON (illuminated). If the QD01/D fails to pass its power-up self-tests, you can select a special diagnostic mode (switch SW2-1 ON) which causes the LED indicators to display an error code. See Self-Test Error Reporting, in Section 5, TROUBLESHOOTING.

During normal operation, LED1 and LED2 flicker occasionally. These LEDs are used to indicate LSI-11 bus activity and ST-506 disk drive activity respectively.

BLANK

5.1 OVERVIEW

This section describes the several diagnostic features with which the QD01/D Disk Controller is equipped, and outlines fault isolation procedures that use these diagnostic features.

Subsection	Title
5.2	Service
5.3	Fault Isolation Procedures
5.4	Power-Up Self-Diagnostics
5.5	Fatal Error Codes

5.2 SERVICE

Your Emulex QD01/D Disk Controller was designed to give years of trouble-free service, and it was thoroughly tested before leaving the factory.

Should one of the fault isolation procedures indicate that the QD01/D is not working properly, the product must be returned to the factory or to one of Emulex's authorized repair centers for service. Emulex products are not designed to be repaired in the field.

Before returning the product to Emulex, whether the product is under warranty or not, you must contact the factory or the factory's representative for instructions and a Return Materials Authorization (RMA) number.

Do not return a component to EMULEX without authorization. A component returned for service without an authorization will be returned to the owner at the owner's expense.

In the continental United States, Alaska, and Hawaii contact:

Emulex Technical Support
3545 Harbor Boulevard
Costa Mesa, CA 92626
(714)662-5600 TWX 910-595-2521

Outside the United States, contact the distributor from whom the subsystem was initially purchased.

To help you efficiently, Emulex or its representative requires certain information about the product and the environment in which it is installed. During installation, a record of the switch setting should have been made on the Configuration Reference Sheet. This sheet is contained in the Installation Section, Figure 4-1.

After you have contacted Emulex and received an RMA, package the component (preferably using the original packing material) and send the component **postage paid** to the address given you by the Emulex representative. The sender must also insure the package.

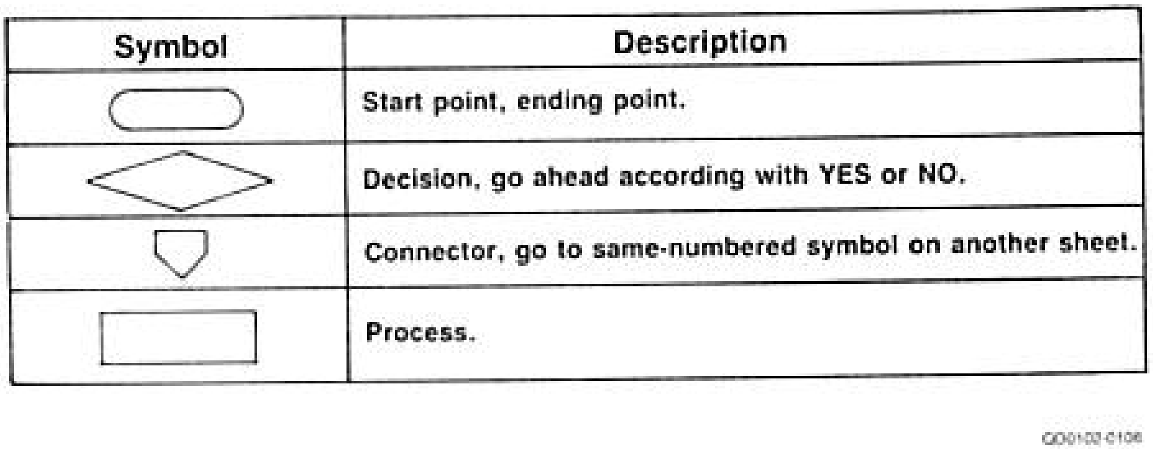
5.3 FAULT ISOLATION PROCEDURE

This fault isolation procedure is provided in flowchart format. The procedure is based on the self-diagnostics incorporated into the QD01/D. The procedure is designed to be used if the product's self-diagnostic fails or if many errors are flagged by the subsystem during normal operation. If neither of these events happens, it is not necessary to follow these procedures.

The Fault Isolation Chart is shown in Figure 5-1. The chart symbols are defined in Table 5-1.

If the fault isolation procedure indicates that a component needs to be returned to Emulex, see subsection 5.2 for instructions on how to do so.

Table 5-1. Flow Chart Symbol Definitions



Symbol	Description
⬭	Start point, ending point.
◇	Decision, go ahead according with YES or NO.
⬠	Connector, go to same-numbered symbol on another sheet.
▭	Process.

QD0102-0106

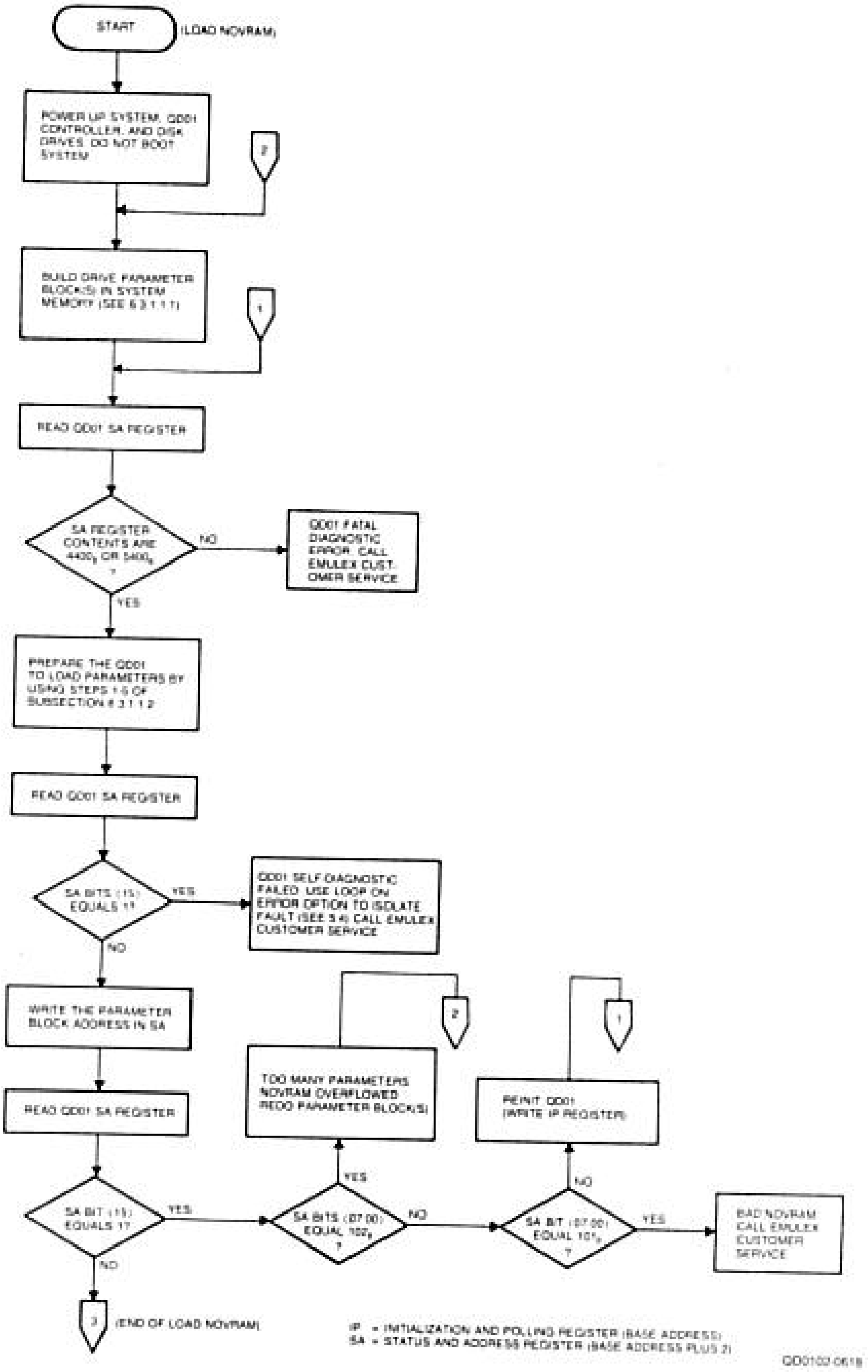
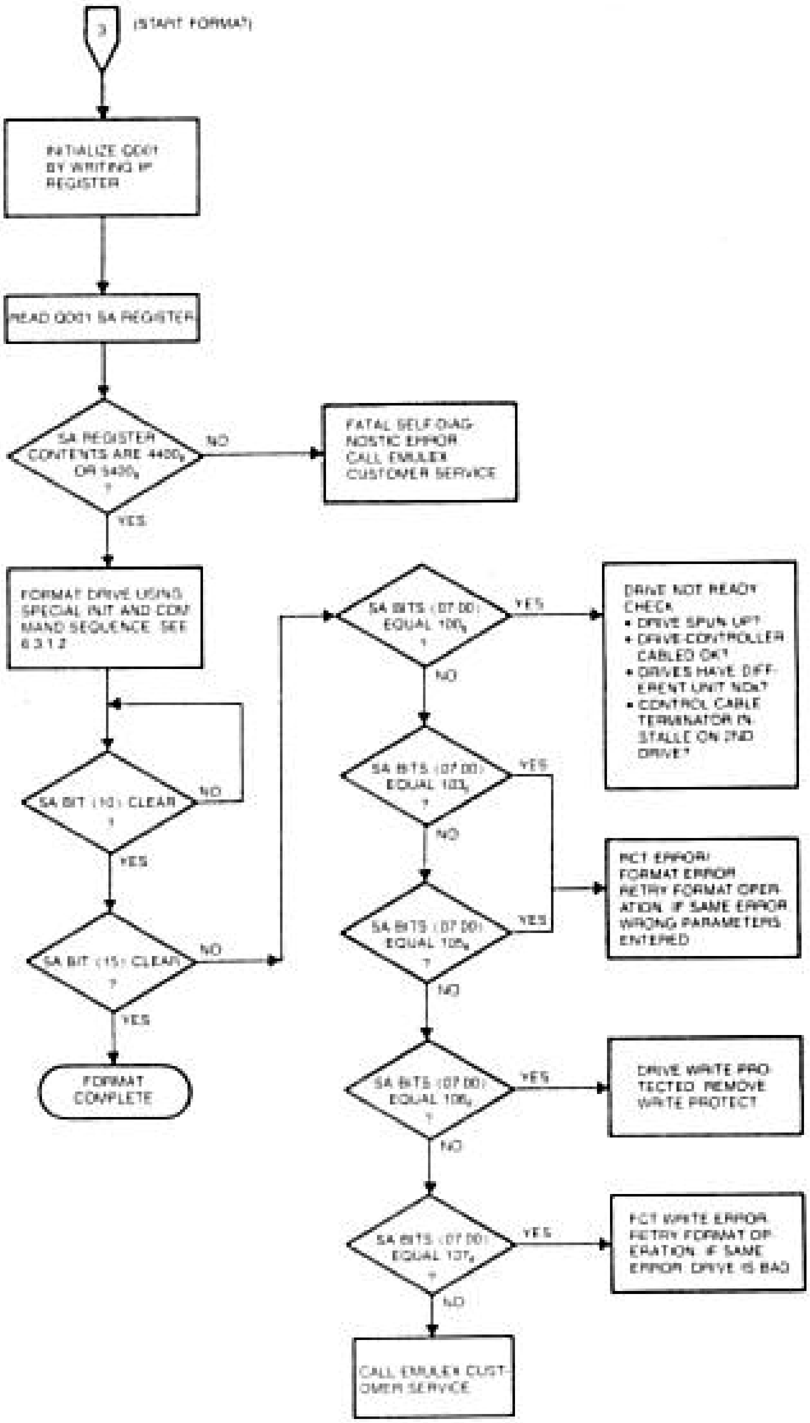

START
(LOAD NOVRAM)
POWER UP SYSTEM, QD01 CONTROLLER, AND DISK DRIVES. DO NOT BOOT SYSTEM
2
BUILD DRIVE PARAMETER BLOCK(S) IN SYSTEM MEMORY (SEE 6.3.1.1.1)
1
READ QD01 SA REGISTER
SA REGISTER CONTENTS ARE 4400_8 OR 5400_8 ?
NO
QD01 FATAL DIAGNOSTIC ERROR. CALL EMULEX CUSTOMER SERVICE
YES
PREPARE THE QD01 TO LOAD PARAMETERS BY USING STEPS 1-5 OF SUBSECTION 6.3.1.1.2
READ QD01 SA REGISTER
SA BITS (15) EQUALS 1?
YES
QD01 SELF DIAGNOSTIC FAILED. USE LOOP ON ERROR OPTION TO ISOLATE FAULT (SEE 5.4) CALL EMULEX CUSTOMER SERVICE
NO
WRITE THE PARAMETER BLOCK ADDRESS IN SA
READ QD01 SA REGISTER
SA BIT (15) EQUALS 1?
YES
SA BITS (07:00) EQUAL 102_8 ?
YES
TOO MANY PARAMETERS NOVRAM OVERFLOWED REDO PARAMETER BLOCK(S)
2
NO
SA BIT (07:00) EQUAL 101_8 ?
NO
REINIT QD01 (WRITE IP REGISTER)
1
YES
BAD NOVRAM CALL EMULEX CUSTOMER SERVICE
NO
3
(END OF LOAD NOVRAM)
IP = INITIALIZATION AND POLLING REGISTER (BASE ADDRESS)
SA = STATUS AND ADDRESS REGISTER (BASE ADDRESS PLUS 2)
QD0102-0618

Figure 5-1. Fault Isolation Chart (sheet 1 of 2)


3
(START FORMAT)
INITIALIZE QD01 BY WRITING IP REGISTER
READ QD01 SA REGISTER
SA REGISTER CONTENTS ARE 4400_8 OR 5400_8 ?
NO
FATAL SELF-DIAGNOSTIC ERROR CALL EMULEX CUSTOMER SERVICE
YES
FORMAT DRIVE USING SPECIAL INIT AND COMMAND SEQUENCE. SEE 6.3.1.2
SA BIT (10) CLEAR ?
NO
YES
SA BIT (15) CLEAR ?
NO
YES
FORMAT COMPLETE
SA BITS (07:00) EQUAL 100_8 ?
YES
DRIVE NOT READY CHECK
• DRIVE SPUN UP?
• DRIVE-CONTROLLER CABLED OK?
• DRIVES HAVE DIFFERENT UNIT NOs?
• CONTROL CABLE TERMINATOR INSTALLED ON 2ND DRIVE?
NO
SA BITS (07:00) EQUAL 103_8 ?
YES
NO
SA BITS (07:00) EQUAL 105_8 ?
YES
RCT ERROR/ FORMAT ERROR RETRY FORMAT OPERATION. IF SAME ERROR WRONG PARAMETERS ENTERED
NO
SA BITS (07:00) EQUAL 106_8 ?
YES
DRIVE WRITE PROTECTED. REMOVE WRITE PROTECT
NO
SA BITS (07:00) EQUAL 107_8 ?
YES
FCT WRITE ERROR RETRY FORMAT OPERATION. IF SAME ERROR DRIVE IS BAD
NO
CALL EMULEX CUSTOMER SERVICE

IP = INITIALIZATION AND POLLING REGISTER (BASE ADDRESS)
SA = STATUS AND ADDRESS REGISTER (BASE ADDRESS PLUS 2)

QD0102-0619

Figure 5-1. Fault Isolation Chart (Sheet 2 of 2)

5.4 POWER-UP SELF-DIAGNOSTIC

The QD01/D executes an extensive self-diagnostic to ensure that the disk controller is in good working order. The self-diagnostic is divided into several parts. Table 5-2 lists the tests in the order in which they are performed.

The first two tests are executed immediately after power-up, a reset, a bus INIT, or a write to the IP register (base address). The other tests are executed as the controller interacts with the MSCP initialization routine. If the QD01/D fails any of the tests, it posts an error code in the SA register (base address plus 2) and turns on all of its status LEDs. There are three LEDs, and they are located on the outside edge of the PWB. The fatal error codes used by the QD01/D are listed in Table 5-3.

To help determine the location of the problem, the operator can select a special diagnostic mode that causes the LEDs to display an error code. To enable this diagnostic mode, place the CPU halt switch in the ON position and set the QD01/D switch SW2-1 ON (1). After setting SW2-1 ON, the host computer must be powered down or QD01/D switch SW1-1 must be toggled (turned ON and then OFF) to cause the QD01/D to again perform its self-test.

Upon encountering an error, the host microprocessor halts and the LEDs display an error code. The error codes are listed and described in Table 5-2.

If the QD01/D completes the diagnostic mode without errors, all three LEDs are OFF. Set switch SW2-1 in the OFF position and reset the QD01/D controller before using.

Table 5-2. Error Codes

LED 3	 2	 1	Error Description
0	0	1	CPU Chip Test failed
0	1	0	Formatter Chip Test failed
1	0	0	Controller idle, waiting for initialization
0	1	1	Buffer Controller or External Memory Test failed
1	0	1	HAC Test failed
1	1	0	RAM Refresh Test failed
1	1	1	Emulation PROM Checksum Test failed
0	0	0	Self-Diagnostic complete without errors.

5.5 FATAL ERROR CODES

If the QD01/D encounters a fatal error anytime during operation, all three LEDs are illuminated and an error code is posted in the low-byte of the SA register (base address plus 2). Table 5-3 lists the fatal error codes used by the QD01/D.

Table 5-3. MSCP Error Codes used by the QD01/D

Octal Code	Hex Code	Description
0	0	No information in message packet.
1	1	Possible parity or timeout error when the QD01/D attempted to read data from a message packet.
2	2	Possible parity or timeout error when the QD01/D attempted to write data to a message packet.
4	4	QD01/D diagnostic self-test indicated a controller RAM error.
5	5	QD01/D diagnostic self-test indicated a firmware checksum error.
6	6	Possible parity or timeout error when the QD01/D attempted to read an envelope address from a command ring.
7	7	Possible parity or timeout error when the QD01/D attempted to write an envelope address to a command ring.
11	9	Host did not communicate with QD01/D within the time frame established while bringing the controller online. (If this code appears during firmware formatting, it indicates a seek timeout.)
12	A	Operating system sent more commands to the QD01/D than the controller can accept.

Table 5-3. MSCP Error Codes used by the QD01/D (continued)

Octal Code	Hex Code	Description
13	B	Controller unable to perform DMA transfer operation correctly.
14	C	QD01/D diagnostic self-test indicated controller fatal error.
16	E	The MSCP connection identifier is invalid.
23	13	An error occurred during the MSCP initialization sequence.

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6.1 OVERVIEW

This section contains an overview of the QD01/D device registers that are accessible to the LSI-11 Bus and that are used to monitor and control the QD01/D Disk Controller. The registers are functionally compatible with DEC implementations of MSCP Controllers.

The following table outlines the contents of this section.

Subsection	Title
6.1	Overview
6.2	Overview of MSCP Subsystem
6.3	Programming
6.4	Registers

6.2 OVERVIEW OF MSCP SUBSYSTEM

Mass Storage Control Protocol (MSCP) is the protocol used by a family of mass storage controllers and devices designed and built by Digital Equipment Corporation. MSCP allows a host system to be connected to subsystems with a variety of capacities and geometries. This flexibility is possible because MSCP defines data locations in terms of sequential, logical blocks, not in terms of a physical description of the data's location (i.e., cylinder, track, and sector). This scheme gives the MSCP subsystem the responsibility for converting MSCP logical block numbers into physical addresses that the peripheral device can understand.

This technique has several implications. First, the MSCP subsystem must have detailed knowledge of the peripheral's capacity, geometry, and status. Second, the ability to make the translation between logical and physical addresses implies considerable intelligence on the part of the subsystem. Finally, the host is relieved of responsibility for error detection and correction because its knowledge of the media is insufficient to allow error control to be done efficiently.

There are several advantages to this type of architecture. First, it provides the host with an "error free" media. Second, it provides for exceptional operating system software portability because, with the exception of capacity, the characteristics of all MSCP subsystems are the same from the operating system's point of view.

In terms of implementation, this protocol requires a high degree of intelligence on the part of the subsystem. Essentially, this intelligence is a process that runs on a microprocessor and is referred to as an MSCP Controller. The MSCP Controller has all of the responsibilities outlined above.

The host computer runs corresponding software processes which take calls from the operating system, convert them into MSCP commands, and cause the resulting command to be transferred to the MSCP Controller.

In summary, an MSCP subsystem is characterized by an intelligent controller that provides the host with the view of a perfect media. It is further characterized by host independence from a specific bus, controller, or device type.

6.3 PROGRAMMING

A complete description of MSCP commands and the corresponding status responses which the QD01/D Disk Controller posts is beyond the scope of this manual. A comprehensive description of MSCP may be ordered from the DEC Software Distribution Center, Order Administration/ Processing, 20 Forbes Rd., Northboro, Massachusetts 01532.

- UDA50 Programmer's Documentation Kit (QP905-GZ). This kit consists of the following three software manuals:
    - MSCP Basic Disk Function Manual (AA-L619A-TK)
    - Storage System Diagnostic and Utilities Protocol (AA-L260A-TK)
    - Storage System UNIBUS Port Description (AA-L621A-TK)

The QD01/D Disk Controller executes the Minimal Disk Subset of MSCP Commands. This subsection contains a description of the extra commands that the QD01/D executes and a list of the MSCP functions that are not supported by the QD01/D Disk Controller.

6.3.1 EXPANDED COMMANDS

The following subsection describes the MSCP-type commands that the QD01/D Disk Controller executes in addition to the Minimal Disk Subset described in the MSCP Basic Disk Functions Manual.

6.3.1.1 Drive Configuration Command

The QD01/D allows the user to specify media geometry for the ST-506 disk drives that it supports. The geometry data is stored in an electrically alterable read-only memory (NOVRAM) on the QD01/D. When used with the QD01/D, the NOVRAM can store configurations for two physical drives.

The NOVRAM is programmed while the QD01/D is installed by loading the drive geometry parameters into the host computer's memory and by executing a command sequence that causes the QD01/D to read those parameters. Both operations can be performed manually by using the CPU console (or a console emulator such as ODT), or automatically by using a special utility that uses the command sequence but does most of the bit toggling. Emulex provides utilities for VAX-11, and PDP-11 and LSI-11 processors: the MicroVAX QD01 MSCP Disk Formatter Program (FQD01M) and the Emulex PDP/LSI MSCP Formatter Program (SXMX8A). See paragraph 1.4, Options, for ordering information.

The following paragraphs describe the geometry parameters that are required, their format, and the command sequence that causes the parameters to be stored in the NOVRAM.

6.3.1.1.1 Drive Geometry Parameters Figure 6-1 shows the format of the parameters and lists them. The following paragraphs explain each parameter.

The parameter information block consists of 16 words of data. Each word contains a drive parameter. A separate block is required for each different type of drive on the controller. There may be only two physical drives. The blocks are placed anywhere in the first 64K of memory and must be contiguous. The first word of the parameter block can be stored at any address; the addresses of subsequent words (and parameter blocks) are contiguous and numerically higher.

NOTE

> For MicroVAX II systems, the first word of the parameter block must be stored at 0.

The first block (lowest numerical address) defines the first drive that is connected to the controller (Drive 0). A second block would define Drive 1. The first word of the block gives the number of drives to which the block applies. If it is the first block and the first word contains a 2, then the block defines drives 0 and 1.

All of the parameters are expressed in binary notation and are right-justified in the cells. The most significant bit (MSB) is 15. Each parameter is described in the following paragraphs.

M 2235 [illegible] oct.

Word	15 14 13 12 11 10 09 08 07 06 05 04 03 02 01 00
1 1	Number of Units of this Type
2 1	Type Code
3 0	Starting Head Offset
4 16	Number of Sectors per Track
5 8	Number of Heads
6 516	Number of Cylinders
7 1	Number of Spare Sectors per Track
8 4	Number of Alternate Cylinders
9 0	Reserved
10 0	Split Code
11 0	Removable Media Flag
12 0	Hard/Soft Sector Flag
13 320	Reduced Write Current Cylinder
14 0	Write Precompensation Cylinder
15 1	Step Code
16 0	Sector Zero Offset

Figure 6-1. Drive Configuration Parameter Block

Number of Units of this Type (1)

This word specifies the number of physical disk drives that this parameter block defines. This number cannot be larger than 2. If this word is 0, then words 1 through 17 are ignored.

Type Code (2)

This word indicates the media type. The only valid entry is 1 to indicate fixed disk media.

Starting Head Offset (3)

This word specifies the physical drive head that is to be used as the first head of the second logical drive. This field has meaning only if a Split Code of 3 (word 11) is specified. For example, if a split code of 3 was specified and the Starting Head Offset was set to 2 for a drive with four heads, then heads 0 and 1 would be used for the first logical drive and 2 and 3 would be used for the second logical drive.

Number of Sectors per Track (4)

This word specifies the number of logical sectors per physical track. Spare sectors are not included in this number. The valid range is from 1 through 63.

Number of Heads (5)

This word specifies the number of data heads per drive. The valid range is from 1 through 16.

Number of Cylinders (6)

This word specifies the number of logical cylinders per physical drive. Spare cylinders are not included in this number. The valid range is from 1 through 4095.

Number of Spare Sectors per Track (7)

This word specifies the number of spare sectors reserved per track. This number plus the number of logical sectors per track (word 3) equals the total number of physical sectors per track. The valid range is 0 or 1. If 0 is specified, no spare sectors are reserved.

Number of Alternate Cylinders (8)

This word specifies the number of spare cylinders per physical drive. This number plus the number of logical cylinders (word 5) equals the total number of physical cylinders. The valid range is from 0 through 127. If 0 is specified, no spare cylinders are reserved. You must reserve two cylinders if spare sectors are specified (the sector replacement algorithm needs the cylinders for working space). A minimum of 2 two cylinders must be specified as alternates. Emulex recommends 2 cylinders for an Atasi and 4 cylinders for a Maxtor drive.

If Split code 1 or 2 is specified, the alternate cylinders are divided evenly between the two logical drives. Therefore, an even number of alternate cylinders should be specified. If split code 3 is specified, the alternate cylinders are divided on a per head basis (as the logical units are).

Reserved (9)

Emulex reserves this word for future use. The only valid value is 0.

Split Code (10)

This word allows the drive defined by this parameter block to be split into two logical disk units (two each, if more than one drive is defined by this block). The relative sizes of the logical drives are defined as follows:

Code	Drive 0	Drive 1
0	8/8	0
1	4/8	4/8
2	7/8	1/8
3	Head Offset Dependent	

Code 0: No split.

Code 1: The cylinders are split evenly between the two logical drives. If there is an odd number of cylinders, the odd cylinder is not used.

Code 2: The total number of cylinders are divided by 8. The first drive contains seven-eighths of the total, and the second contains one-eighth. When the number of cylinders is not evenly divisible by eight, the odd cylinders (remainder of the division) are assigned to the larger logical unit.

Code 3: The drive's data heads are divided between the two logical drives. See Starting Head Offset, word 2.

Use of the split option disables seek-ordering and overlapped seek processing in the MSCP Server, which reduces performance, particularly when both logicals of a split physical drive are active. Therefore, we do not recommend using this option unless necessary to allow for convenient file backup and restoration.

Removable Media (11)

This word uses a 2-bit field for physical drive units and uses a 4-bit field for split or mapped logical drives. For a 2-bit field, bit 0 of this word indicates whether the disk media is fixed or removable. Clearing (0) bit 0 indicates fixed media. Setting (1) bit 0 indicates removable media. For a 4-bit field, 1 indicates fixed media and 2 indicates removable media.

Hard or Soft Sectored (12)

Bit 0 of this word indicates whether the disk drive is hard or soft sectored. As all ST-506 drives are currently soft sectored, the QD01/D always interprets this bit as 0. No other values are valid.

Reduced Write Current Cylinder (13)

This word specifies the physical cylinder at which the write current to the data heads is reduced. Some disk drives require that the write current to the heads be reduced above a certain cylinder to reduce the strength of the flux transition. This reduction prevents adjacent flux transitions in the higher cylinders (where they are closer together) from displacing one another to such an extent as to force data bits out of their data clock windows.

Consult the drive manufacturer's technical manual for the proper cylinder. The valid range is from 0 through 4096. If no reduction is required, specify the total number of physical cylinders.

Write Precompensation Cylinder (14)

This word specifies the physical cylinder at which the timing of write data transmitted to the disk drive must be advanced or retarded (with reference to the disk data clock). This timing shift compensates for timing shifts that are caused by adjacent flux transitions in the higher cylinders (where they are closer together). Shifting the write data with respect to the data clock ensures that, when the data is read back, the data will fall within the clock window, despite the tendency of one transition to affect the apparent position of the adjacent transition. This shifting is called precompensation.

Consult the drive manufacturer's technical manual for the proper cylinder. The valid range is from 0 through 4096. If no precompensation is required, specify the total number of physical cylinders.

Write data is precompensated by 12 nanoseconds (both early and late).

Step Code (15)

Bits 0 and 1 of this word are used to specify one of four head stepping codes:

Code	Stepping Timing	Technique
0	3 msec	Non-buffered
1	13.2 usec	Buffered
2	30 usec	Buffered
3	Reserved	

Timing: This number indicates the rate at which step pulses are transmitted to the disk drive.

Technique: This term indicates whether or not the QD01/D expects the drive to buffer step pulses (i.e., to accept pulses faster than it can execute them). Actually, timing is what is being specified, but because few drives can seek faster than 3 msec cylinder to cylinder, shorter pulse intervals assume that the drive is buffering pulses.

Sector Zero Offset (16)

This word specifies the number of sectors by which sector 0 is offset from sector 0 of the previous cylinder. Offsetting sector 0 from one cylinder to the next is a technique that is used to reduce latency when performing write or read operations that cross a cylinder boundary. When the drive is formatted, sector 0 of a cylinder is offset a certain number of sectors from the position of sector 0 on the previous cylinder. When this is done, spiral write and read operations are more efficient because the drive has time to seek from cylinder to cylinder before encountering sector 0. The number of sectors by which to offset is computed by using the following procedure:

1. Find the number of sectors that pass under the drive heads per millisecond using this formula:

$$\frac{\text{Spindle Speed (RPM)} \times \text{Sectors per Track}}{60{,}000} = \text{Sectors per msec}$$

2. Compare the sectors per millisecond with the cylinder-to-cylinder seek time for your drive:

$$\text{Sectors per msec} \times \text{Cylinder-Cylinder Seek Time} = \text{Sectors per Seek}$$

3. Round the Sectors per Seek figure up to the next integer, add 1 and round up to the next even integer. Divide that even number by 2, and use the dividend as the Sector Zero Offset.

The valid range for this field is 0 through number of sectors divided by 2. If no offset is desired, specify 0.

6.3.1.1.2 Loading the NOVRAM A special sequence of commands causes the QD01/D to load the parameter blocks from memory into the NOVRAM. The process uses the Initializing and Polling (IP) register (QD01/D base address) and the Status and Address (SA) register (base address plus 2). (See section 6.4 for register octal and hexadecimal notation.) To load the NOVRAM on a MicroVAX II, you must first prepare the system for DMA transfer operations:

1. Apply power to the system and initialize the LSI-11 bus by depositing 0 in internal memory register 37. If you have a running system, you must bring it down before executing this step.

   ```
   >>>D/I 37 0<return>
   ```

2. Enable external access to local memory by loading 20_{16} into the Interprocessor Communications Register (ICR) at address $20001F40_{16}$:

   ```
   >>>D/P/W 20001F40 20<return>
   ```

3. Set the map register for the first page in memory to 0 by depositing 80000000_{16} in map register 20088000_{16}:

   ```
   >>>D/P/L 20088000 80000000<return>
   ```

4. Proceed to step 1 of the NOVRAM command sequence. Be sure to store the NOVRAM parameters at memory location 0.

The NOVRAM command sequence is as follows:

1. Initialize the QD01/D by writing any value into the IP register. The QD01/D performs its self-test and begins the initialization dialog.

Register	Octal	Hexadecimal
IP: Host Write	000001	0001

2. The QD01/D indicates that initialization step 1 has begun by setting bit 11 in the SA register. The host must poll the register for this value (no interrupt is generated). Bit 8 should also be set. If 22-bit addressing is enabled, bit 9 will be set.

Register	Octal	Hexadecimal	Addressing
SA: Host Read	004400 005400	0900 0B00	18-Bit 22-Bit

3. When the controller indicates that step 1 of the initialization dialog is begun, load the SA register with the "special initialization code:"

Register	Octal	Hexadecimal
SA: Host Write	030003	3003

4. The controller acknowledges the initialization code with: 00400.

Register	Octal	Hexadecimal
SA: Host Read	000400	0100

5. Write the Define Unit Geometry command into the SA register:

Register	Octal	Hexadecimal
SA: Host Write	041000	4200

6. The QD01/D finishes its self-test (about two seconds) before acknowledging with:

Register	Octal	Hexadecimal
SA: Host Read	001000	0200

   You must wait until the QD01/D acknowledges before proceeding.

7. Write the 16-bit memory address of the first word of the first parameter block into the SA register.

   For example, if you loaded the first word of the first parameter block at memory address 001000:

Register	Octal	Hexadecimal
SA: Host Write	001000	0200

8. The QD01/D begins loading the parameter blocks. Word 17 of the last parameter block must be 0 to indicate that there is no more data (Word 17 would be the first word of the next parameter block, if there was another).

   After the QD01/D has stored the parameter data in the NOVRAM, it reads the data from the NOVRAM and computes a one-byte checksum. It places the checksum in the SA register. The host knows that the checksum is available when bit 09 of SA is clear (0).

   If the QD01/D sets SA bit 15 after it clears bit 09, an error has occurred. The low byte contains the error code.

Error Code		Description
101_8	41_{16}	Check sum error (NOVRAM may be bad)
102_8	42_{16}	NOVRAM capacity exceeded (too many parameters)

6.3.1.2 Format Drive Command

The QD01/D also has the ability to format the disk drives attached to it. This format operation is performed autonomously by the QD01/D in response to a special initialization command. The process uses the IP and SA registers (see section 6.4 for register octal and hexadecimal notation.) To initiate the format operation, use the following procedure.

1. Initialize the QD01/D by writing any value into the IP register. The QD01/D performs self-test and begins the initialization dialog.

Register	Octal	Hexadecimal
IP: Host Write	000001	0001

2. The QD01/D indicates that initialization step 1 has begun by setting bit 11 in the SA register. The host must poll the register for this value (no interrupt is generated). Bit 8 should also be set. If 22-bit addressing is enabled, bit 9 will be set.

Register	Octal	Hexadecimal	Addressing
SA: Host Read	004400 005400	0900 0B00	18-Bit 22-Bit

3. When the controller indicates that step 1 of the initialization dialog is begun, load the SA register with the "special initialization code:"

Register	Octal	Hexadecimal
SA: Host Write	030003	3003

4. The controller acknowledges the initialization code with 00400.

Register	Octal	Hexadecimal
SA: Host Read	000400	0100

5. Write the Format Unit command into the SA register:

Register	Octal	Hexadecimal
SA: Host Write	0420nn	440n

where n is the number of the logical unit to be formatted. Valid values for n range from 0 to 8. If the logical drive is supported by an alternate QD01/D controller, add the unit offset specified by switches SW1-2 through SW1-4.

6. The QD01/D acknowledges the command with:

Register	Octal	Hexadecimal
SA: Host Read	001000	0200

7. Write the 16-bit volume serial number into the SA register. This number may be any value from 1 to 177777_8 ($FFFF_{16}$).

Register	Octal	Hexadecimal
SA: Host Write	000001	0001

8. The QD01/D acknowledges the serial number with:

Register	Octal	Hexadecimal
SA: Host Read	002000	0400

9. Write the format parameter word into the SA register. (The format parameter word is not defined and is reserved for future use. Write all zeros into the register.) The QD01/D begins formatting the selected drive.

Register	Octal	Hexadecimal
SA: Host Write	000000	0000

10. Poll the SA register until the QD01/D clears SA bit 10 to indicate that the format operation concluded. If the operation was not successful, the QD01/D sets bit 15 in the SA register. The low byte of the register contains the error code:

Error Octal	Code Hex	Description
100	40	Drive not ready
103	43	RCT Write error
105	45	Format error
106	46	Drive write protected
107	47	FCT Write error

6.3.1.3 Bootstrap Command

To allow the system to be easily bootstrapped from peripherals attached to the QD01/D Disk Controller, Emulex has incorporated a Bootstrap Command into the controller. This feature is not part of the standard MSCP command set nor is it supported on the MicroVAX or on systems using an 11/73B CPU module.

The Bootstrap Command can be issued from the console after the system is powered up, or it may be incorporated into a firmware routine that is located in a Bootstrap ROM. (The ROM would not be located on the QD01/D PWB, but on some other module in the system.)

The Bootstrap Command causes the QD01/D to load the first logical block from the selected peripheral into host memory starting at location 00000.

To issue the Bootstrap Command to the QD01/D, load the SA register with the following values (see section 6.4 for register octal and hexadecimal notation):

1. 030003_8 or 3003_{16}

2. $0400nn_8$ or $400n_{16}$, where n is the MSCP logical unit number (see Section 3).

No other operation can be performed between the loading of the two numbers. After issuing the command to the QD01/D, CPU registers R0 and R1 must be loaded with the unit number and the CSR address of the QD01/D, respectively.

Figure 6-2 is an example of the Bootstrap Command as issued from the system console under Console ODT. The QD01/D's base address is 172150_8 and the MSCP logical unit number is zero. The system output is displayed in normal type; the operator input is displayed in **boldface.** The QD01/D registers must contain the indicated patterns. However, the patterns indicated for the contents of R0 and R1 are only examples; the initial contents of those registers (before the unit number and address are loaded) may be anything.

```
@772150/00000<lf>           !<lf>=LINE FEED/<cr>=RETURN
772152/005400 30003<cr>     !4400 not 5400 if 18-bit
@/000400 40000<cr>          !Now wait for SA to go to 0
@R0/103741 0<lf>
R1/001276 772150<cr>
@0G
```

Figure 6-2. Bootstrap Command Example

6.3.2 UNSUPPORTED COMMANDS

No currently available MSCP Server supports the entire range of MSCP commands. The following subsections list and describe the MSCP commands that the QD01/D does not support.

6.3.2.1 Minimal Disk Subset

The QD01/D MSCP Server supports the entire minimal disk subset of MSCP.

6.3.2.2 Diagnostic and Utility Protocol (DUP)

The QD01/D MSCP Server does not support any of the DUP commands or maintenance read/write commands.

6.4 REGISTERS

During normal operation, the QD01/D MSCP Server is controlled and monitored using the command and status packets that are exchanged by the Class Driver (host) and the MSCP Server. The QD01/D has two 16-bit registers in the LSI-11 Bus I/O page that are used primarily to initialize the subsystem. During normal operation, the registers are used only to initiate polling or to reset the subsystem. These registers are always read as words. The register pair begins on a longword boundary. Table 6-1 lists the octal and hexadecimal values for Initialization and Polling (IP) register (base address) and the Status, Address and Purge (SA) register (base address plus 2) supported by the QD01/D.

Table 6-1. IP and SA Registers

Register	Octal	Hexadecimal
IP SA	772150 772152	20001468 2000146A
IP SA	772154 772156	2000146C 2000146E
IP SA	760334 760336	200000DC 200000DE
IP SA	760340 760342	200000E0 200000E2
IP SA	760344 760346	200000E4 200000E6
IP SA	760350 760352	200000E8 200000EA
IP SA	760354 760356	200000EC 200000EE
IP SA	760360 760362	200000F0 200000F2

The IP register has two functions as detailed below:

- When written with any value, it causes a hard initialization of the MSCP Server.
- When read while the port is operating, it causes the controller to initiate polling.

The SA register has four functions as listed below:

- When read by the host during initialization, it communicates data and error information relating to the initialization process.
- When written by the host during initialization, it communicates certain host-specific parameters to the port.
- When read by the host during normal operation, it communicates status information including port- and controller-detected fatal errors.
- When zeroed by the host during either initialization or normal operation, it signals the port that the host has successfully completed a bus adapter purge in response to a port-initiated purge request.

The detailed operation of these registers is discussed in the Storage System UNIBUS Port Description (AA-L621A-TK) available from DEC as described in subsection 6.3. Note that only word transfers to and from IP and SA are permissible; the behavior of byte transfers is undefined.

7.1 OVERVIEW

This section contains a description of the QD01/D Disk Controller's architecture. The following table outlines the contents of this section.

Subsection	Title
7.1	Overview
7.2	QD01/D Controller Architecture

7.2 QD01/D DISK CONTROLLER ARCHITECTURE

The QD01/D is a microprocessor-based emulating disk controller that is contained on a single dual-wide PCBA. The QD01/D major functional blocks are shown in Figure 7-1. The disk controller is organized around the eight-bit 8031 microprocessor. The board has an eight-bit internal data bus with 16-bit addressing capability. The Host Adapter Controller, the Formatter Controller, and the Buffer Controller are addressed as memory (memory-mapped I/O).

The 8031's primary task is to decode and implement commands from the host. At command completion, the microprocessor is also responsible for generating status and transmitting it to the host. A large part of the microprocessor's job while performing those duties involves setting up the Host Adapter Controller and the Buffer Controller for the large data transfers that are their specialties.

The QD01/D has 16K bytes of erasable programmable read-only memory (EPROM), which contains the control program, and 16K bytes of random access memory (RAM), which is used for data buffering and working storage.

The LSI-11 bus interface contains 22 lines. Sixteen of the lines are multiplexed for both address and data; six are used for only address. The Host Adapter Controller is used for programmed I/O, CPU interrupts, and DMA data transfers. The microprocessor responds to all programmed I/O and carries out the I/O functions required for the addressed disk controller register. The Host Adapter Controller has automatic LSI-11 bus address generation capability that, in conjunction with a byte counter, allows the interface to conduct LSI-11 bus DMA transfers without direct microprocessor intervention after the interface is set up for a transfer. This automatic DMA capability is used with the QD01/D Buffer Controller to transfer large blocks of data directly between host memory and the QD01/D's RAM.

The Buffer Controller is implemented on a single chip. This multi-channel controller is responsible for moving large blocks of data between the 16K RAM buffer and the ST-506 interface, and between the LSI-11 bus interface and the 16K RAM buffer. After being set up for an operation by the microprocessor, either interface requests DMA service from the Buffer Controller by driving an individual request signal active. The transfer then proceeds without direct intervention by microprocessor. This allows high-speed data transfers to occur while the microprocessor is focused on other processes.

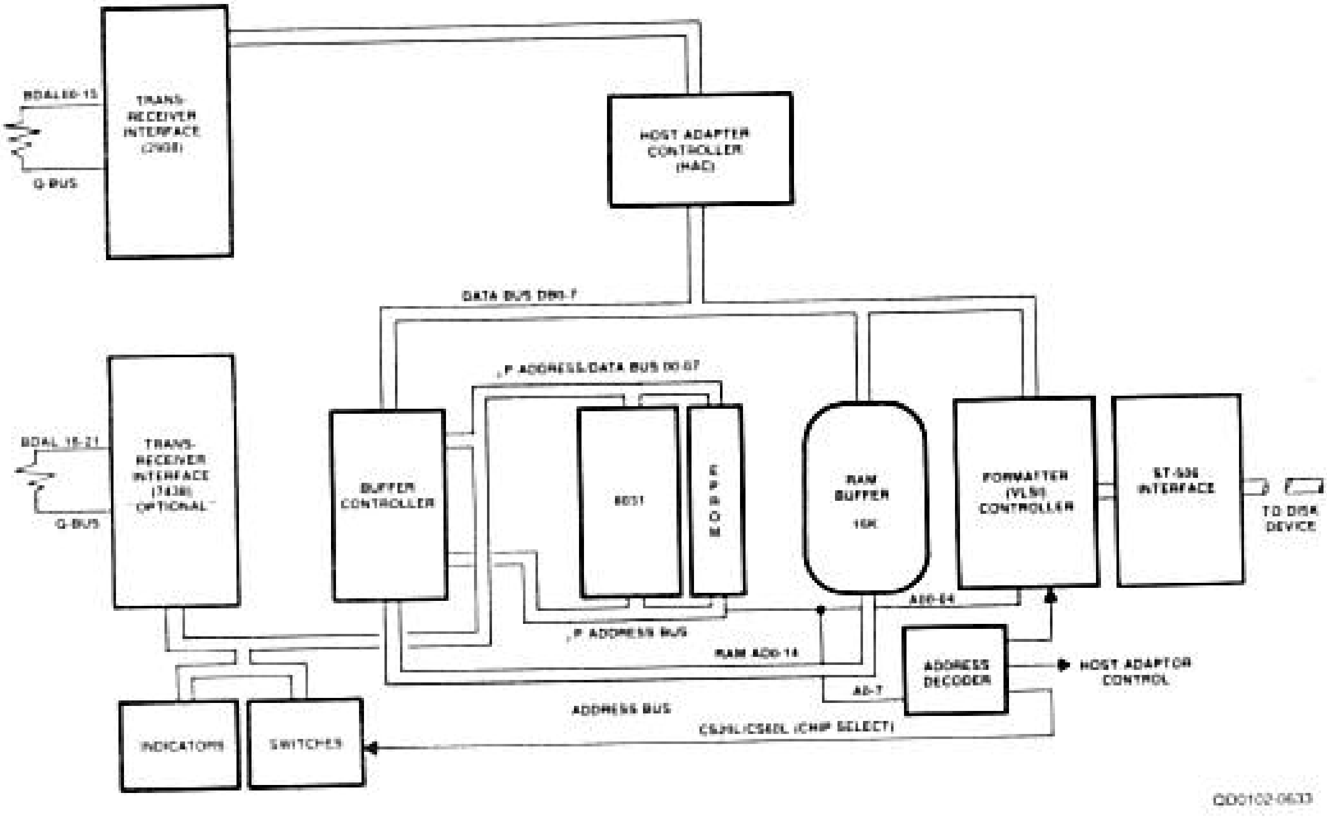


Figure 7-1. QD01/D Block Diagram

Section 8
INTERFACES

8.1 OVERVIEW

This section describes the interfaces that the QD01/D Disk Controller incorporates. It includes information on the QD01/D implementation of ST-506 interface electrical and mechanical requirements. Excluding this overview, the section is divided into the following subsections.

Subsection	Title
8.2	QD01/D LSI-11 Bus Interface
8.3	QD01/D ST-506 Drive Interface

8.2 LSI-11 BUS INTERFACE

The LSI-11 bus between the LSI-11 CPU and the QD01/D Disk Controller contains 42 bidirectional signal lines and two unidirectional signal lines on connectors A and B, and two unidirectional signal lines on connector C. LSI-11 bus interface pin assignments are listed and described in Table 8-1. These signal lines provide the means by which the LSI-11 CPU and the QD01/D Disk Controller communicate with each other.

The LSI-11 bus interface is used for programmed I/O, CPU interrupts, and NPR Data Transfer operations. Addresses, data, and control information are sent along these signal lines, some of which contain time-multiplexed information. The LSI-11 bus interface lines are grouped in the following categories:

- **Twenty-two Data/Address Lines** <BDAL00:BDAL21> The four Data/Address lines which carry the most significant bits (MSB) are lines BDAL21:BDAL18. They are used for addressing only and do not carry data. Lines BDAL17 and BDAL16 reflect the parity status of the 16-bit data word during a Write or Read Data Transfer operation via the LSI-11 bus cycle.
- **Six Data Transfer Control Lines** BBS7, BDIN, BDOUT, BRPLY, BSYNC, and BWTBT.
- **Six Direct Memory Access (DMA) Control Lines** BDMR, BSACK, BDMGI, and BDMGO (connectors A and C).
- **Seven Interrupt Control Lines** BEVNT, BIAKI, BIAKO, BIRQ4, BIRQ5, BIRQ6, and BIRQ7.
- **Five System Control Lines** BDCOK, BHALT, BINIT, BPOK, and BREF.

Table 8-1. LSI-11 Bus Interface Pin Assignments

Connector A Signal			Connector B Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
BIRQ5	A	+5V	BDCOK	A	+5V
BIRQ6	B		BPOK	B	
BDAL16	C	0V (GND)	BDAL18	C	0V (GND)
BDAL17	D		BDAL19	D	
	E	BDOUT	BDAL20	E	BDAL02
	F	BRPLY	BDAL21	F	BDAL03
	H	BDIN		H	BDAL04
0V (GND)	J	BSYNC	0V (GND)	J	BDAL05
	K	BWTBT		K	BDAL06
	L	BIRQ4		L	BDAL07
0V (GND)	M	BIAKI	0V (GND)	M	BDAL08
BDMR	N	BIAKO	BSACK	N	BDAL09
BHALT	P	BBS7	BIRQ7	P	BDAL10
BREF	R	BDMGI	BEVNT	R	BDAL11
	S	BDMGO		S	BDAL12
0V (GND)	T	BINIT	0V (GND)	T	BDAL13
	U	BDAL00		U	BDAL14
	V	BDAL01		V	BDAL15

Connector C Signal			Connector D Signal		
Component Side	Pin	Solder Side	Component Side	Pin	Solder Side
	A	+5V		A	+5V
	B			B	
	C	0V (GND)		C	0V (GND)
	D			D	
	E			E	
	F			F	
	H			H	
0V (GND)	J		0V (GND)	J	
	K			K	
	L			L	
0V (GND)	M	BIAKI	0V (GND)	M	
	N	BIAKO		N	
	P			P	
	R	BDMGI		R	
	S	BDMGO		S	
0V (GND)	T		0V (GND)	T	
	U			U	
	V			V	

All signals, except BDCOK and BPOK, are low active.

8.2.1 INTERRUPT PRIORITY LEVEL

The QD01/D is hardwired to issue both level 4 and level 5 interrupt requests. The level 4 request is necessary to allow compatibility with either an LSI-11 or LSI-11/2 CPU.

8.2.2 REGISTER ADDRESS

The QD01/D Disk Controller has two registers visible to the LSI-11 bus. Their addresses are determined by DIP switches SW2-3 through SW2-5. See Section 4 for detailed address and switch setting information.

8.2.3 DMA OPERATIONS

All DMA Data Transfer operations are performed under microprocessor control. When doing a Read or Write From Memory operation, a check is made for memory parity errors or Non-Existent Memory (NXM) errors. If an error is detected, an MSCP status error is returned.

8.2.4 SCATTER/GATHER

The QD01/D Disk Controller supports the MicroVAX I I/O technique of scatter-write operations and gather-read operations.

8.3 QD01/D ST-506 DISK DRIVE INTERFACE

The QD01/D Controller interfaces with each ST-506 disk drive via a 34-pin control cable and one of two 20-pin data cables. A 34-pin male connector at reference designator J1 on the QD01/D Controller plugs directly into the ST-506 disk drive control cable. The QD01/D Controller contains two 20-pin male connectors, one at reference designator J2 and one at reference designator J5

The QD01/D Controller can control a maximum of two disk drives. Either 20-pin connector (reference designator J2 or J5) can plug directly into the data cable for the first disk drive. If a second disk drive is configured, the unused 20-pin connector is plugged into the data cable for that disk drive.

Figure 8-1 shows the pin/signal assignments for control signal interface between the QD01/D Controller and an ST-506 disk drive. The control signal interface has a maximum cable length of 20 feet. Figure 8-2 shows the pin/signal assignments for data signal interface between the QD01/D Controller and an ST-506 disk drive. The data signal interface also has a maximum cable length of 20 feet.

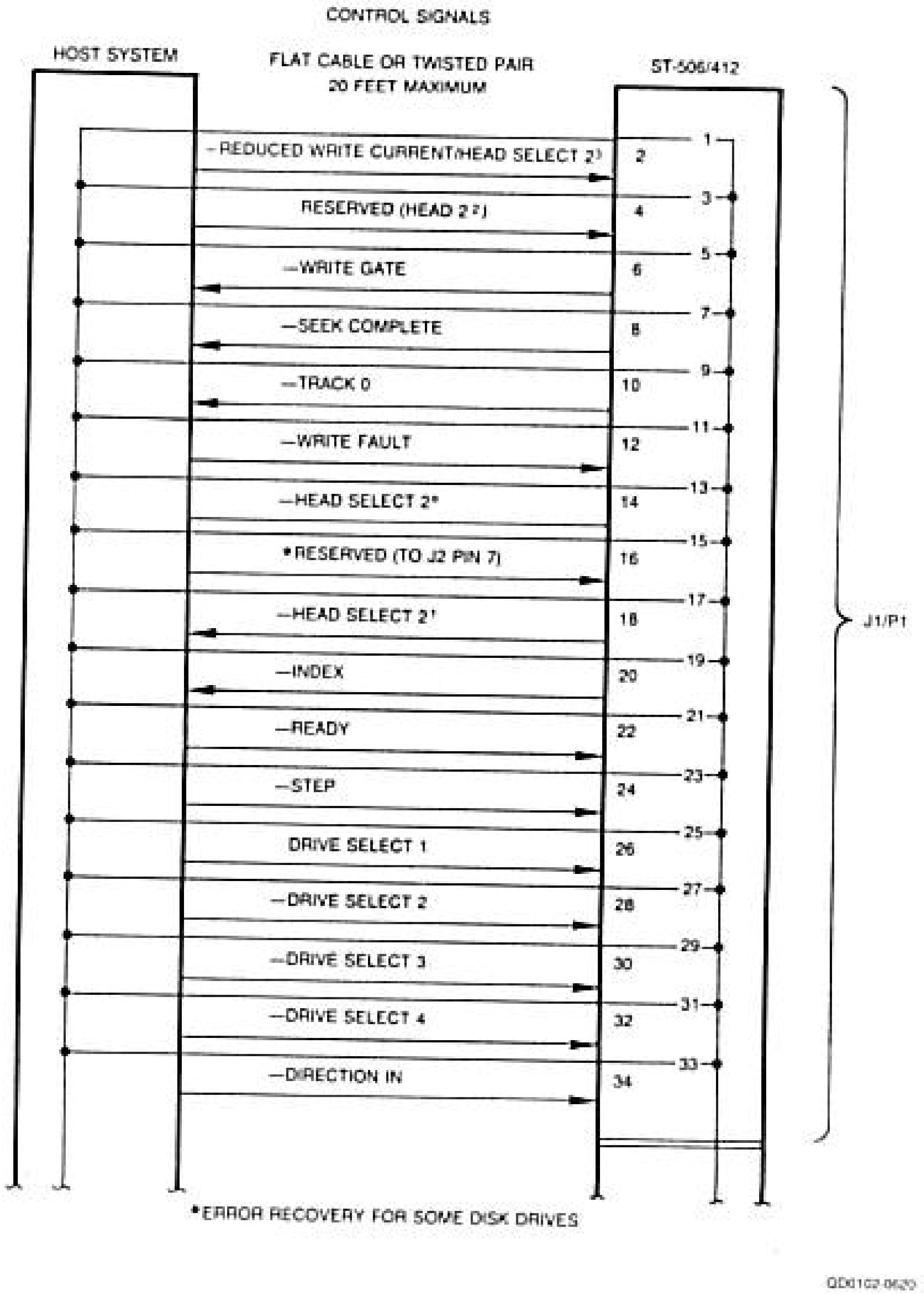
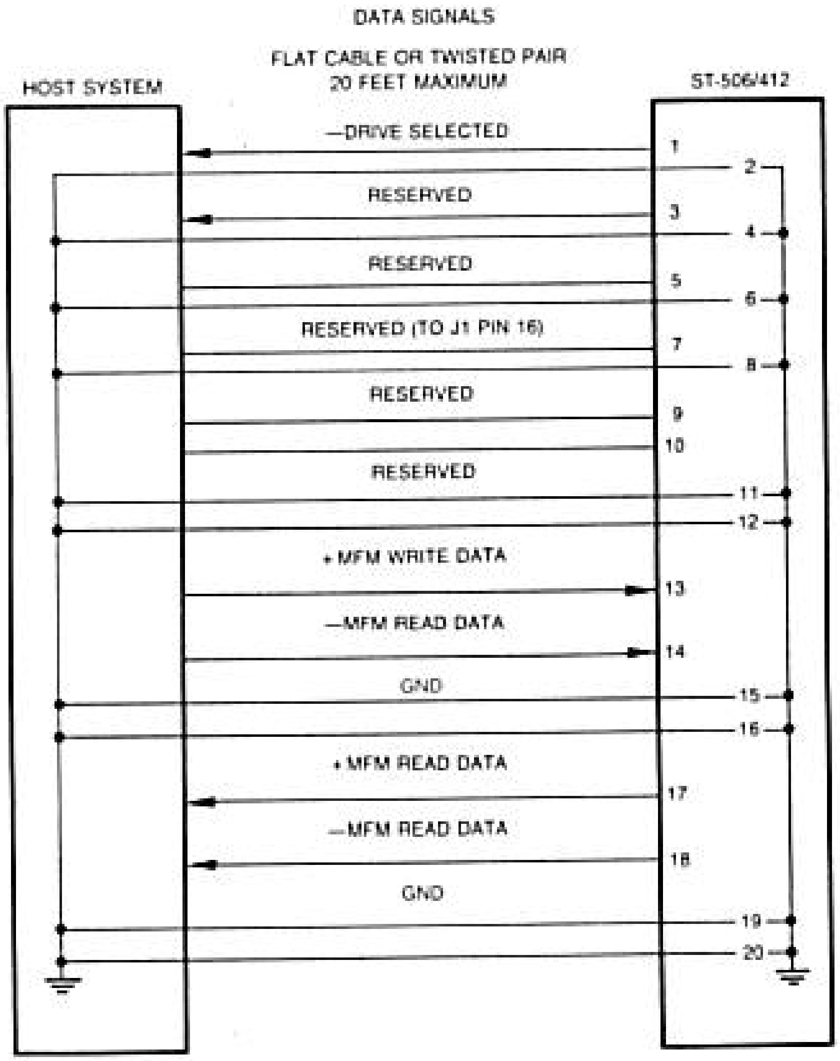


Figure 8-1. Control Pin/Signal Assignments at ST-506 Disk Drive Interface (Connector P1)



QD0102-0621

Figure 8-2. Data Pin/Signal Assignments at ST-506 Disk Drive Interface (Connector J2 or J5)

8.4 FRONT PANEL INTERFACE

The QD01/D provides an interface that allows a remote control and status panel to be connected to the controller. The interface allows write protect switches for each ST-506 drive to be connected, and it provides drivers for ready and write-protected status LEDs.

The interface is implemented by using a four-wall, right-angle header (3M part number 3591-5002) designated J3 The header has 10 pins. The function of each pin is described in Table 8-2. Figure 8-3 shows the pin-outs and a sample user interface.

Table 8-2. Control and Status Interface Pin Function Description

Pin	Function	Description
1	Ground	Controller Logic Ground
2	Not Connected	
3	Disk 1 Write Protect Input	Ground this line to write protect disk 1
4	Disk 1 Ready Status	This line sinks 24 mA when disk 1 is ready
5	Disk 0 Write Protect Input	Ground this line to write protect disk 0
6	Disk 0 Ready Status	This line sinks 24 mA when disk 0 is ready
7	Disk 1 Write Protect Status	This line sinks 24 mA when disk 1 is write protected
8	Not connected	
9	Disk 0 Write Protect Status	This line sinks 24 mA when disk 0 is write protected
10	+5 VDC	This line provides 5 VDC. This line is not current protected.

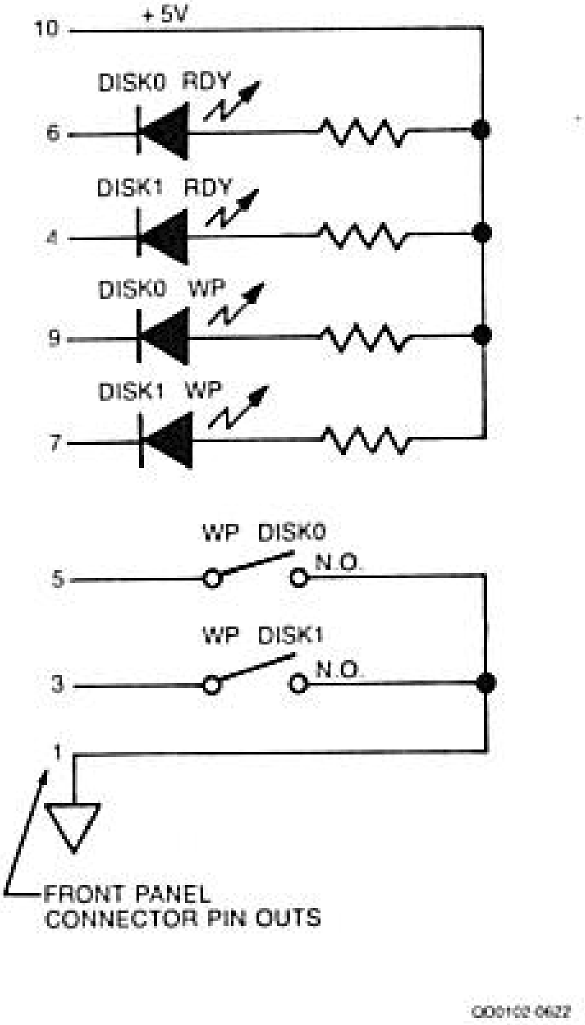


Figure 8-3. Status and Control Interface

Appendix A
AUTOCONFIGURE, CSR and VECTOR ADDRESSES

A.1 OVERVIEW

The following discussion presents the algorithm for assignment of floating addresses and vectors for all DEC operating systems. Bus addresses are discussed in subsection 3.3.2.

A.2 DETERMINING THE CSR ADDRESS FOR USE WITH AUTOCONFIGURE

The term Autoconfigure refers to a software utility that is run when the computer is bootstrapped. This utility finds and identifies I/O devices in the I/O page of system memory.

Some devices (like the DM11) have fixed addresses reserved for them. Autoconfigure detects their presence by simply testing their standard address for a response. Specifically, the control/status register (CSR) address, which is usually the first register of the block, is tested.

Addresses for those devices not assigned fixed numbers are selected from the floating CSR address space (760010 - 763776) of the Unibus input/output (I/O) page. This means that the presence or absence of floating devices will affect the assignment of addresses to other floating-address devices. Similarly, many devices have floating interrupt vector addresses. According to the DEC standard, vectors must be assigned in a specific sequence and the presence of one type of device will affect the correct assignment of vectors for other devices.

The CSR address for a floating-address device is selected according to the algorithm used during autoconfigure. The algorithm is used in conjunction with a Device Table, Table A-1.

Essentially, Autoconfigure checks each valid CSR address in the floating CSR address space for the presence of a device. Autoconfigure expects any devices installed in that space to be in the order specified by the Device Table. Also, the utility expects an eight-byte block to be reserved for each device that is not installed in the system. Each empty block tells Autoconfigure to look at the next valid address for the next device on the list.

When a device is detected, a block of addresses is reserved for the device according to the number of registers it employs. The utility then looks at the next CSR for that device type. If there is a device there, it is assumed to be of the same type as the one before it and a block is reserved for that device. If there is no response at the next address, that space is reserved to indicate that there are no more devices of that type. Then the utility checks the CSR address (at the appropriate boundary) for the next device in the table.

Table A-1. SYSGEN Device Table

Rank	Device	Number of Registers	Octal Modulus	Rank	Device	Number of Registers	Octal Modulus
1	DJ11	4	10	17	Reserved	4	10
2	DH11	8	20	18	RX11[2]	4	10
3	DQ11	4	10	18	RX211[2]	4	10
4	DU11,DUV11	4	10	18	RXV11[2]	4	10
5	DUP11	4	10	18	RXV21[2]	4	10
6	LK11A	4	10	19	DR11-W	4	10
7	DMC11	4	10	20	DR11-B[3]	4	10
7	DMR11	4	10	21	DMP11	4	10
8	DZ11[1]	4	10	22	DPV11	4	10
8	DZV11	4	10	23	ISB11	4	10
8	DZS11	4	10	24	DMV11	8	20
8	DZ32	4	10	25	DEUNA[2]	4	10
9	KMC11	4	10	26	UDA50[2]	2	4
10	LPP11	4	10	27	DMF32	16	40
11	VMV21	4	10	28	KMS11	6	20
12	VMV31	8	20	29	VS100	8	20
13	DWR70	4	10	30	TU81	2	4
14	RL11[2]	4	10	31	KMV11	8	20
14	RLV11[2]	4	10	32	DHV11	8	20
15	LPA11-K[2]	8	20	33	DMZ32	16	40
16	KW11-C	4	10	34	CP132	16	40

[1] DZ11-E and DZ11-F are treated as two DZ11s.

[2] The first device of this type has a fixed address. Any extra devices have a floating address.

[3] The first two devices of this type have a fixed address. Any extra devices have a floating address.

In summary, there are four rules that pertain to the assignment of device addresses in floating address space:

1. Devices with floating addresses must be attached in the order in which they are listed in the Device Table, Table A-1.

2. The CSR address for a given device type is assigned on word boundaries according to the number of Unibus- accessible registers that the device has. The following table relates the number of device registers to possible word boundaries.

Device Registers	Possible Boundaries
1	Any Word
2	XXXXX0, XXXXX4
3,4	XXXXX0
5,6,7,8	XXXX00,XXXX20,XXXX40,XXXX60
9 thru 16	XXXX00,XXXX40

   The Autoconfigure utility inspects for a given device type only at one of the possible boundaries for that device. That is, the utility does not look for a DMF32 (16 registers) at an address that ends in 20.

3. An 8-byte gap must follow the register block of any installed device to indicate that there are no more of that type of device. This gap must start on the proper CSR address boundary for that type of device.

4. An 8-byte gap must be reserved in floating address space for each device type that is not installed in the current system. The gap must start on the proper word boundary for the type of device the gap represents. That is, a single DJ11 installed at 760010 would be followed by a gap starting at 760020 to show a change of device types. A gap to show that there are none of the next device on the list, a DH11, would begin at 760040, the next legal boundary for a DH11-type device.

A.3 DETERMINING THE VECTOR ADDRESS FOR USE WITH AUTOCONFIGURE

There is a floating vector address convention that is used for communications and other devices which interface with the Unibus. These vector addresses are assigned in order starting at 300 and proceeding upwards to 777. Table A-2 shows the assignment sequence. For a given system configuration, the device with the highest floating vector rank would be assigned to vector address 300. Additional devices of the same type would be assigned subsequent vector addresses according to the number of vectors required per device, and according to the starting boundary assigned to that device type.

Table A-2. Priority Ranking for Floating Vector Addresses (starting at 300 and proceeding upwards)

Rank	Device	Number of Vectors	Octal Modulus
1	DC11	2	10
1	TU58	2	10
2	KL11[1]	2	10
2	DL11-A[1]	2	10
2	DL11-B[1]	2	10
2	DLV11-J[1]	8	40
2	DLV11,DLV11-F[1]	2	10
3	DP11	2	10
4	DM11-A	2	10
5	DN11	1	4
6	DM11-BB/BA	1	4
7	DH11 modem control	1	4
8	DR11-A, DRV11-B	2	10
9	DR11-C, DRV11	2	10
10	PA611 (reader+punch)	4	20
11	LPD11	2	10
12	DT07	2	10
13	DX11	2	10
14	DL11-C to DLV11-F	2	10
15	DJ11	2	10
16	DH11	2	10
17	VT40	4	20
17	VSV11	4	10
18	LPS11	6	40
19	DQ11	2	10
20	KW11-W, KWV11	2	10
21	DU11, DUV11	2	10
22	DUP11	2	10
23	DV11 + modem control	3	20
24	LK11-A	2	10
25	DWUN	2	10
26	DMC11	2	10
26	DMR11	2	10
27	DZ11/DZS11/DZV11	2	10
27	DZ32	2	10
28	KMC11	2	10
29	LPP11	2	10

(continued on next page)

Table A-2. Priority Ranking for Floating Vectors Addresses (starting at 300_8 and proceeding upwards) (continued)

Rank	Device	Number of Vectors	Octal Modulus
30	VMV21	2	10
31	VMV31	2	10
32	VTV01	2	10
33	DWR70	2	10
34	RL11/RLV11[2]	1	4
35	TS11[2], TU80[2]	1	4
36	LPA11-K	2	10
37	IP11/IP300[2]	1	4
38	KW11-C	2	10
39	RX11[2]	1	4
39	RX211[2]	1	4
39	RXV11[2]	1	4
39	RXV21[2]	1	4
40	DR11-W	1	4
41	DR11-B[2]	1	4
42	DMP11	2	10
43	DPV11	2	10
44	ML11[3]	1	4
45	ISB11	2	10
46	DMV11	2	10
47	DEUNA[2]	1	4
48	UDA50[2]	1	4
49	DMF32	8	40
50	KMS11	3	20
51	PCL11-B	2	10
52	VS100	1	4
53	Reserved	1	4
54	KMV11	2	10
55	Reserved	2	10
56	IEX	2	10
57	DHV11	2	10
58	DMZ32	6	20
59	CP132	6	20

[1] A KL11 or DL11 used as a console, has a fixed vector.

[2] The first device of this type has a fixed vector. Any extra devices have a floating vector.

[3] ML11 is a Massbus device which can connect to a UNIBUS via a bus adapter.

Vector addresses are assigned on the boundaries indicated in the modulus column of Table A-2. That is, if the modulus is 10, then the first vector address for that device must end with zero (XX0). If the modulus is 4, then the first vector address can end with zero or 4 (XX0, XX4).

Vector addresses always fall on modulo 4 boundaries (XX0, XX4). That is, a vector address never ends in any number but four or zero. Consequently, if a device has two vectors and the first must start on a modulo 10 boundary, then, using 350 as a starting point, the vectors will be 350 and 354.

A.4 A SYSTEM CONFIGURATION EXAMPLE

Table A-3 contains an example of a system configuration that includes devices with fixed addresses and vectors, and floating addresses and/or vectors.

Table A-4 shows how the device addresses for the floating address devices in Table A-3 were computed, including gaps.

Table A-3. CSR and Vector Address Example

Controller	Vector	CSR
1 UDA50	154	772150
1 DZ11	300	760100
1 UDA50	310	760354
2 DHV11	320	760500
	330	760520

Table A-4. Floating CSR Address Assignment Example

Installed	Device		Octal Address
	DJ11	Gap	760010
	DH11	Gap	760020
	DQ11	Gap	760030
	DU11	Gap	760040
	DUP11	Gap	760050
	LK11A	Gap	760060
	DMC11	Gap	760070
---->	DZ11		760100
		Gap	760110
	KMC11	Gap	760120
	LPP11	Gap	760130
	VMV21	Gap	760140
	VMV31	Gap	760150
	DWR70	Gap	760170
	RL11	Gap	760200
	LPA11-K	Gap	760220
	KW11-C	Gap	760230
	Reserved	Gap	760240
	RX11	Gap	760250
	DR11-W	Gap	760260
	DR11-B	Gap	760270
	DMP11	Gap	760300
	DPV11	Gap	760310
	ISB11	Gap	760320
	DMV11	Gap	760340
	DEUNA	Gap	760350
---->	UDA50 (QD01/D)		772150[1]
---->	UDA50 (QD01/D)		760354
		Gap	760360
	DMF32	Gap	760400
		Gap	760440
	KMS11	Gap	760420
	VS100	Gap	761440
	TU81	Gap	761450
	KMV11	Gap	761460
---->	DHV11		761500
---->	DHV11		761520
		Gap	761530
	DMZ32	Gap	761540
	CP132	Gap	761600

[1] Fixed address

B.1 OVERVIEW

This appendix provides instructions for replacing the QD01/D's firmware PROM.

B.2 EXCHANGING PROMS

The QD01/D firmware PROM is located in the socket at U43. Remove the existing PROM from its socket using an IC puller or an equivalent tool.

The QD01/D PROM is identified by the part numbers on top of the PROMS (A62). Place the QD01/D PROM in socket U43. Make certain that the PROM is firmly seated and that no pins are bent or misaligned. (If the two rows of PROM pins are too far apart to fit in the socket, grasp the PROM at its ends using your thumb and forefinger and bend one of the pin rows inward by pressing it against a table top or other flat surface.)

Table B-1. QD01/D PROM Location

PROM Number	PCBA Location
A62	U43

BLANK

C.1 OVERVIEW

This appendix contains a list of the diagnostics and utilities software that are available for use with the QD01/D. The list includes a description of the function of the software and a description of the media on which the software is distributed. The media and supporting documentation are supplied in diagnostic distribution kits as described in Table C-1.

All of the diagnostic and utility media listed contain all of the software provided for the QD01/D by Emulex.

Table C-1. Utility and Diagnostic Software

Part Number	Media Type	Boot Type	Description
PX9951801-01	0.5-inch tape, 800 bpi	MT	All tape, disk, communications, and subsystem software
PX9951801-02	0.5-inch tape, 1600 bpi	MT	All tape, disk, communications, and subsystem software
PX9951801-03	0.5-inch tape, 1600 bpi	MS	All tape, disk, communications, and subsystem software
PX9951801-04	0.25-inch cartridge tape	MS	All tape, disk, communications, and subsystem software
PX9951802-01	IOMEGA disk cartridge	DL	Emulex Subsystem software (subset of above)
PX9951802-02	0.25-inch cartridge tape	MS	Emulex Subsystem software (subset of above)

continued next page

Table C-1. Utility and Diagnostic Software (continued)

Part Number	Media Type	Boot Type	Description
PX9951802-03	IOMEGA Disk Cartridge	DU	Emulex Subsystem software (subset of above)
VX9951804	RX50 Floppy	DU	MicroVAX Diagnostics

Appendix D
DISK DRIVE CONFIGURATION PARAMETERS

D.1 OVERVIEW

This appendix contains tables that give the configuration parameters for common ST-506 disk drives. These tables give only parameters relating to the physical geometry of the disk drives; options such as logical splits are left to the user (see subsection 6.3.1.1.).

Tables D-1 through D-6 list the parameters in octal for PDP/LSI, hexadecimal for MicroVAX, and decimal as an additional reference for Emulex software. These parameters are based on the following assumptions:

- One spare sector per track
- Four spare cylinders per disk
- No logical splits are required
- No spiral offsets are required

Table D-1. Maxtor

Word	Dec	Oct	Hex	Description
1	1	1	1	Number of Drives
2	1	1	1	Type Code
3	0	0	0	Head Offset
4	16	20	10	Sectors per Track
5	15	17	F	Heads
6	914	1622	392	Cylinders
7	1	1	1	Spare Sectors per Track
8	4	4	4	Spare Cylinders
9	0	0	0	Reserved
10	0	0	0	Split Code
11	0	0	0	Removable Media Flag
12	0	0	0	Hard/Soft Sector Flag
13	918	1626	396	Reduced Write Current Cylinder
14	918	1626	396	Write Precompensation Cylinder
15	1	1	1	Step Pulse Code
16	0	0	0	Spiral Offset

PDP/LSI Checksum	VAX Checksum
223_8	9316

Table D-2. ATASI 3046

Word	Dec	Oct	Hex	Description
1	1	1	1	Number of Drives
2	1	1	1	Type Code
3	0	0	0	Head Offset
4	16	20	10	Sectors per Track
5	7	7	7	Heads
6	641	1201	281	Cylinders
7	1	1	1	Spare Sectors per Track
8	4	4	4	Spare Cylinders
9	0	0	0	Reserved
10	0	0	0	Split Code
11	0	0	0	Removable Media Flag
12	0	0	0	Hard/Soft Sector Flag
13	320	500	140	Reduced Write Current Cylinder
14	320	500	140	Write Precompensation Cylinder
15	1	1	1	Step Pulse Code
16	0	0	0	Spiral Offset

PDP/LSI Checksum	VAX Checksum
316_8	CE_{16}

QDQ1

Table D-5. Quantum 540 / RD52

Word	Dec	Oct	Hex	Description
1	1	1	1	Number of Drives
2	1	1	1	Type Code
3	0	0	0	Head Offset
4	16	20	10	Sectors per Track
5	8	10	8	Heads
6	508	774	1FC	Cylinders
7	1	1	1	Spare Sectors per Track
8	4	4	4	Spare Cylinders
9	0	0	0	Reserved
10	0	0	0	Split Code
11	0	0	0	Removable Media Flag
12	0	0	0	Hard/Soft Sector Flag
13	512	1000	200	Reduced Write Current Cylinder
14	256	400	100	Write Precompensation Cylinder
15	1	1	1	Step Pulse Code
16	0	0	0	Spiral Offset

PDP/LSI Checksum	VAX Checksum
135_8	$5D_{16}$

Table D-6. Micropolis 13250 / RD 53

Word	Dec	Oct	Hex	Description
1	1	1	1	Number of Drives
2	1	1	1	Type Code
3	0	0	0	Head Offset
4	16	20	10	Sectors per Track
5	8	10	8	Heads
6	1020	1774	3FC	Cylinders
7	1	1	1	Spare Sectors per Track
8	4	4	4	Spare Cylinders
9	0	0	0	Reserved Landing Zone ...
10	0	0	0	Split Code
11	0	0	0	Removable Media Flag
12	0	0	0	Hard/Soft Sector Flag
13	1024	2000	400	Reduced Write Current Cylinder
14	1024	2000	400	Write Precompensation Cylinder
15	1	1	1	Step Pulse Code
16	0	0	0	Spiral Offset

PDP/LSI Checksum	VAX Checksum
53_8	$2B_{16}$

NOTE

If you are using a console emulator to specify only one drive, the next memory location must be zero to signify the end of the parameter block.

Table D-3. Fujitsu M2243AS

Word	Dec	Oct	Hex	Description
1	1	1	1	Number of Drives
2	1	1	1	Type Code
3	0	0	0	Head Offset
4	17 16	20	10	Sectors per Track
5	11	13	B	Heads
6	754 750	1356	2EE	Cylinders
7	1	1	1	Spare Sectors per Track
8	4	4	4	Spare Cylinders
9	0	0	0	Reserved
10	0	0	0	Split Code
11	0	0	0	Removable Media Flag
12	0	0	0	Hard/Soft Sector Flag
13	754	1362	2F2	Reduced Write Current Cylinder
14	0	0	0	Write Precompensation Cylinder
15	1	1	1	Step Pulse Code
16	0	0	0	Spiral Offset

PDP/LSI Checksum	VAX Checksum
274_8	BC_{16}

162_8 bei 2 M2243!

Table D-4. RODIME

Word	Dec	Oct	Hex	Description
1	1	1	1	Number of Drives
2	1	1	1	Type Code
3	0	0	0	Head Offset
4	16	20	10	Sectors per Track
5	8	10	8	Heads
6	636	1174	27C	Cylinders
7	1	1	1	Spare Sectors per Track
8	4	4	4	Spare Cylinders
9	0	0	0	Reserved
10	0	0	0	Split Code
11	0	0	0	Removable Media Flag
12	0	0	0	Hard/Soft Sector Flag
13	640	1200	280	Reduced Write Current Cylinder
14	0	0	0	Write Precompensation Cylinder
15	1	1	1	Step Pulse Code
16	0	0	0	Spiral Offset

PDP/LSI Checksum	VAX Checksum
306_8	C616